empowering communication

Application note

Single-Pair Ethernet with netX 90

Implementation of 10BASE-T1L SPE with netX 90 using external PHY

Hilscher Gesellschaft für Systemautomation mbH

www.hilscher.com

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1 Introduction

1.1 About this document

This application note describes the usage of the netX 90 SoC with a 10BASE-T1L Single Pair Ethernet PHY from Analog Devices.

This application note covers the basics of the Single-Pair Ethernet physical layer as well as the connection from the netX 90 SoC to the PHY via the Media Independent Interface (MII) and the MDIO Interface. Furthermore, the hardware design considerations of using an ADIN1100 together with a netX 90 SoC are described using NXEB 90-SPE evaluation board.

1.2 List of revisions

Rev	Date	Name	Chapter	Revision
1	2021-11-12	MMA	all	Initial revision, document created.
2	2023-11-07	HHE	7.2.1	Section *External MII in combination with SDRAM*: TXCLK added to Table 13.
3	2024-11-01	HHE	all	Use case: Single-Port SPE

Table 1: List of revisions

1.3 Terms, abbreviations and definitions

Term	Description
DPM	Dual-Port Memory
IEC	International Electromechanical Commission
IEEE	Institute of Electrical and Electronics Engineers
MAC	Media Access Controller
MDC	MDIO interface Clock
MDI	Media Dependent Interface
MDIO	Management Data Input/Output
MII	Media Independent Interface
MIIMU	Media Independent Interface Management Unit
MMD	MDIO Manageable Device
PHY	Physical Layer Transceiver
PoDL	Power over Data Line
(R)GMII	(Reduced) Gigabit Media Independent Interface
SoC	System on Chip
SPE	Single-Pair Ethernet
xC Channel	Flexible Communication Channel

Table 2: Terms, abbreviations and definitions

1.4 References to documents

This document refers to the following documents:

[1] IEEE Standards Association, Standard: IEEE Standard for Ethernet, IEEE802.3-2018, English.

[2] IEEE Standards Association, Standard: IEEE Standard for Ethernet, Amendment 5: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors, IEEE802.3cg-2019, English.

[3] Belden, Whitepaper: Single-Pair Ethernet im industriellen Einsatz, German, 2019.

[4] Pepperl+Fuchs, Presentation: 10 Mb/s Single Twisted Pair Ethernet, PAM-3 PHY Baseline Proposal, English, 2017-05.

[5] Analog Devices, Datasheet: Robust, Industrial, Low Power 10BASE-T1L Ethernet PHY, ADIN1100, Rev. PrG, English, 2021.

[6] Würth, Application note: Single-Pair Ethernet für Anwendungen im Industriebereich, ANP085a, German, 2021-03.

[7] Analog Devices, Application note: Evaluating the ADIN1100 Robust, Industrial, Low Power 10BASE-T1L Ethernet PHY, UG-XXXX, Rev. PrB, English, 2020.

[8] Namur, Position paper: An Ethernet communication system for the process industry, English, 2016-02.

[9] Hilscher Gesellschaft für Systemautomation mbH: Technical data reference guide, netX 90, DOC160609TRG09EN, English, 2024-07.

[10] Hilscher Gesellschaft für Systemautomation mbH: Device description, NXEB 90-SPE, 10BASE-T1L Evaluation board, DOC2110001HW04EN, English, 2024-11.

Table 3: References to documents

2 Introduction to netX 90

The netX 90 SoC is the smallest highly integrated industrial Ethernet node in Hilscher's line-up of multi-protocol capable SoC platforms in the netX family. Among other features, it incorporates two ARM Cortex-M4 cores, an on-chip Flash, integrated Ethernet PHYs for 10/100 Mbit/s Standard Ethernet as well as numerous peripherals and an SDRAM controller. The block diagram in Figure 1 shows a high-level overview of the SoC.

By using two ARM cores, netX 90 allows to separate communication and application tasks logically. The communication side additionally features two flexible communication channels (xC channels), which support all popular industrial Ethernet standards. Typically, the xC channels are connected to the internal dual PHYs, but can also be used in combination with external PHYs to further extend the SoCs connectivity to different physical layers of Ethernet-based networks.Furthermore, the XC architecture can be flexibly adapted to new standards via software, making the netX 90 ready for the future.

Hilscher offers loadable firmware (LFW) solutions for the netX 90 also as single endpoint communication device. The NXEB 90-SPE evaluation board enables users to evaluate the functionality of single endpoint devices as rapid prototyping platform for all major physical layers.

The netX 90 is available in a 10 mm x 10 mm 144-pin BGA package.

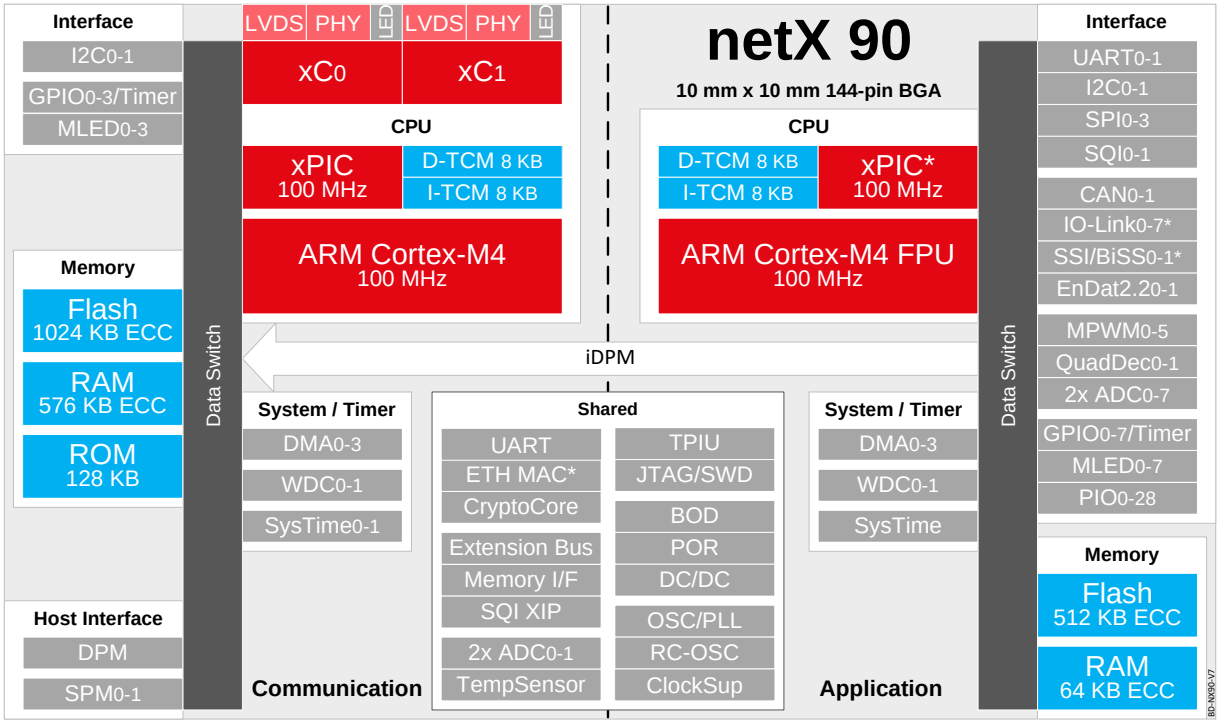

Figure 1: netX 90 SoC block diagram

3 Evaluation board

This application note focuses on the NXEB 90-SPE evaluation board, which is Hilscher's approach towards the development of long-range 10BASE-T1L Single-Pair Ethernet in industrial applications. Figure 2 shows the NXEB 90-SPE evaluation board.

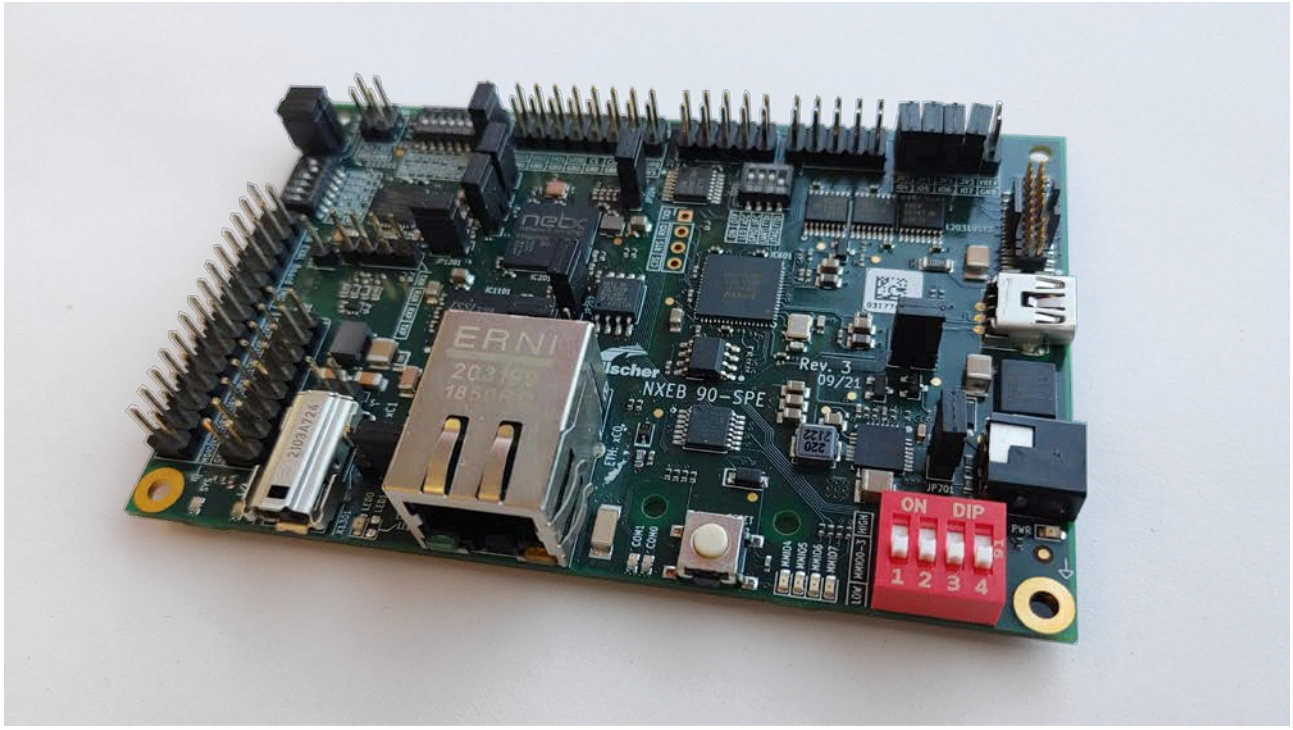

Figure 2: NXEB 90-SPE evaluation board

This evaluation board is designed to evaluate and test the functionality of SPE in industrial applications.

The NXEB 90-SPE board enables users to evaluate the functionality of single endpoint devices as rapid prototyping platform for all major physical layers:

10BASE-T/100BASE-TX standard Ethernet port with RJ45 connector:
Port 0 of the chip internal real-time Ethernet PHY

10BASE-T1L Single Pair Ethernet port with Harting T1 connector:
External ADIN1100 PHY connected to MII1 signals

Fieldbus transceiver connector for CAN, PROFIBUS, and so on:
External transceiver IC connected to MX0 signals

It also demonstrates how to design a generic hardware for all major physical layers with partial PCB assemblies to reduce the number of PCB variants for applications and products.

The layout is based on the standard NXHX 90-JTAG board and thus features almost identical functionality for programming, debugging as well as user I/O. Further features, besides the connectivity, include an on-board 8 MByte SDRAM as well as current measurement points for a variety of components.

Key features:

- 10BASE-T1L SPE support with external ADIN1100 PHY and IEC 63171-6 industrial connector
- 10BASE-T / 100BASE-TX support with RJ45 connector
- Debugging via on-board USB debugger or external JTAG adapter
- Ready for CAN, PROFIBUS, DeviceNet, CC-Link via legacy fieldbus connector
- UART via RS232 adapter or via on-board USB with virtual COM port
- Serial DPM interface for netX 90 companion chip use-cases
- On-board 8 MByte SD-RAM and 4 MByte SQI Flash
- Test points for power measurements of various components

Applications:

- Evaluation of single endpoint communication
- Evaluation of 10SPE/APL communication
- Evaluation of fieldbus communication

Limitations:

- No PoDL (Power over data-line) circuit support for ADIN1100
- No parallel dual-ported memory (DPM) host interface support
- No host interface (HIF) connector for NXHX extension modules

4 Single-Pair Ethernet

This section provides a brief overview on Single-Pair Ethernet (SPE). As a new physical layer for the Ethernet defined in specification IEEE802.3, SPE uses only one pair of conductors to transmit and receive Ethernet frames.

The requirements for an Ethernet communication system based on a single pair of conductors were introduced by *Namur's* position paper back in 2016 (reference [8]). This paper gives an overview of the requirements the process industry has when it comes to field-level Ethernet communication, like cable reach, EMC and explosion protection, power, transmission speeds, etc. It furthermore calls for protocols like PROFINET or EtherNet/IP, which are also currently used in the factory automation world, to become a minimum requirement for SPE communication. Since then, the IEEE picked up the development of various SPE variants in order to standardize the physical layers in the IEEE802.3 Ethernet standard.

This document will focus on the **10BASE-T1L** variant of SPE, which was released by the IEEE in 2019 as amendment IEEE802.3cg to the Ethernet standard.

4.1 Physical layer

The physical layer defines the transmission medium that is used, which in case of SPE is the one-pair cable. The PHY acts as the interface between SPE and the Media Access Controller (MAC). It handles modulation, demodulation and encoding of the data from and to the physical layer, as shown in Figure 3 (on page 8).

The PHY contains the circuitry needed to decode or encode the differential signal on the SPE cable, which is connected to the Media Dependent Interface (MDI), to its raw data form. The data is then passed via the Media Independent Interface (MII) to higher levels for further processing (according to the OSI reference model to an IEEE802.3 compatible MAC).

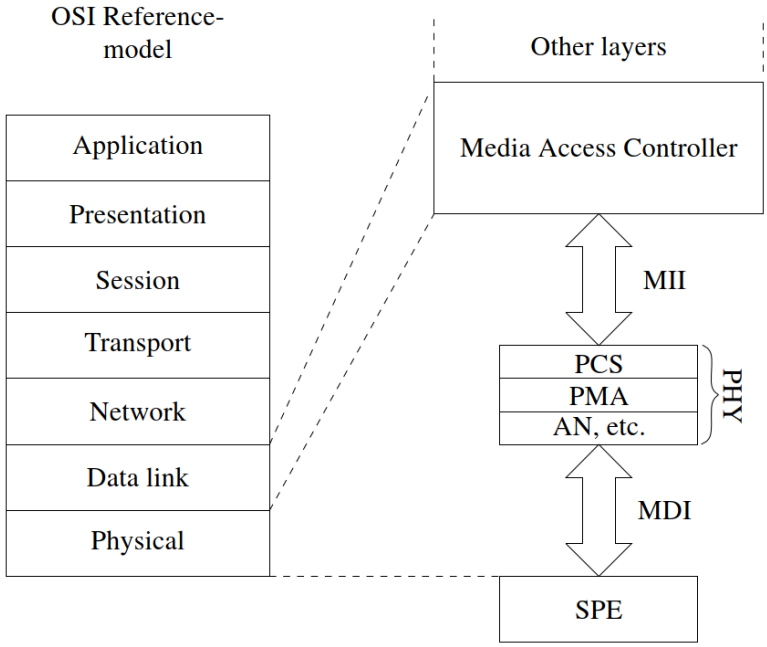

Figure 3: Position of the PHY in respect to the OSI reference model

4.1.1 Electrical signal characteristics and encoding

Data on the MDI will be transmitted with PAM3 modulation, which has three logical signal levels: $-V_{MDI}$, 0 and V_{MDI}. This provides good distinguishability between the different symbol levels after long distances [4].

The IEEE802.3cg furthermore defines two possible signal amplitudes (V_{MDI}). 1V pk-pk, which is intended for intrinsic safe applications when supported by the PHY, and 2.4 V pk-pk, which can be used for segments up to 1000 m.

The data stream coming from the MII is encoded with the 4-Binary-3-Ternary (4B3T) encoding. It represents four bits using a code group of three signal pulses. This allows the representation of $2^4 = 16$ different input combinations with $3^3 = 27$ different code groups. To keep the signal free from accumulating a DC offset over time, some combination of input bits can be encoded in different ways, depending on an accumulated *disparity* value. This removes the need for a baseline wander compensation, as used in 10BASE-T or 100BASE-TX, to keep the signal free from DC offsets [2].

Using the 4B3T encoding lowers the total bandwidth from 10 MBaud/s to 7.5 MBaud/s while transmitting 10 Mbit/s of data.

4.1.2 Plugs and cables

Other than traditional Multi-Pair Ethernet (MPE) which commonly uses RJ45 connectors, SPE does not have a standard interface defined yet. The International Electromechanical Commission (IEC) released standard IEC 63171-5 and IEC 63171-6 which defines multiple mating faces for SPE in industrial applications (MICE class 2 and 3).

The MDI interface used on Hilscher's NXEB 90-SPE evaluation board is the *Harting T1 industrial* interface in its MICE class 2 (IP20) variant. No standard SPE connector is in use by many manufactures.

The requirements for cabling depend on the type of SPE used. For 10BASE-T1L, the IEC specifies standards *IEC 61156-13* for fixed and *IEC 61156-14* for flexible installation (for example when using drag-chains) of one-pair symmetric cabling. Among other things, it specifies the parameters for insertion-loss and return-loss over a frequency range of up to 20 MHz [3].

4.2 External PHY ADIN1100

The table below lists the Analog Device ADIN1100 external PHY for 10BASE-T1L which complies fully with the IEEE802.3cg standard. Hilscher's NXEB 90-SPE evaluation board uses this external PHY.

-	**Analog Devices ADIN1100 [5]**
Type	10BASE-T1L 1-port transceiver
Cable reach	▪ 1700 m with 1.0 V pk-pk ▪ 1700 m with 2.4 V pk-pk
Intrinsic safety possible?	Yes, with 1 V pk-pk transmit mode only
Interface to MAC	MII, RMII, RGMII
Package	6 mm x 6 mm, 40-pin LFCSP
IO voltage levels	1.8 V, 2.5 V, 3.3 V
Power supply configurations	Single, dual, and triple supply
Power consumption	▪ 1.0 V dual supply: min. 39 mW ▪ 1.0 V single supply: min. 45 mW ▪ 2.4 V triple supply: min. 75 mW ▪ 2.4 V single supply: min. 109 mW
Temperature range	-40 °C to 105 °C
IEEE1588 SOP detection	Yes: ▪ MII mode: no TX_SOP / RX_SOP ▪ RMII mode: TX_SOP mux'ed to TX_ER pin, RX_SOP mux'ed to RXD_2 pin ▪ RGMII mode: TX_SOP mux'ed to TX_ER pin, no RX_SOP
Other features	▪ Auto-Negotiation ▪ SOP detection for IEEE1588 ▪ Frame generator and checker ▪ Multiple loopback modes including PMA loopback for testing ▪ IEEE test mode support ▪ Two independent LED outputs ▪ Media converter mode ▪ Cable diagnostics (listed as feature, but **not** described in datasheet)

Table 4: Analog Devices PHY parameters for 10BASE-T1L

Note: For netX 90 the 10 MBit/s Single-Pair Ethernet (10SPE) communication firmware (COM LFW), you can use the ADIN1100 only as external PHY. The ADIN1100 has been verified and approved by Hilscher. The firmware uses parameters and settings which fits to the ADIN1100. You cannot use another external PHY for SPE. A second source for the ADIN1100 is not yet available, but in preparation.

5 Interfaces

This chapter describes the different interfaces used in the hardware design.

5.1 Media independent interface (MII)

The MII is defined in IEEE802.3 and describes the interface between the PHY and the MAC. It serves as an independent, full-duplex capable interface to the physical layer and supports 10 Mbit/s and 100 Mbit/s link speeds.

5.1.1 Electrical connections

The MII consists of a four-bit wide data bus in both directions as well as control signals for transmission status information as shown in Figure 4.

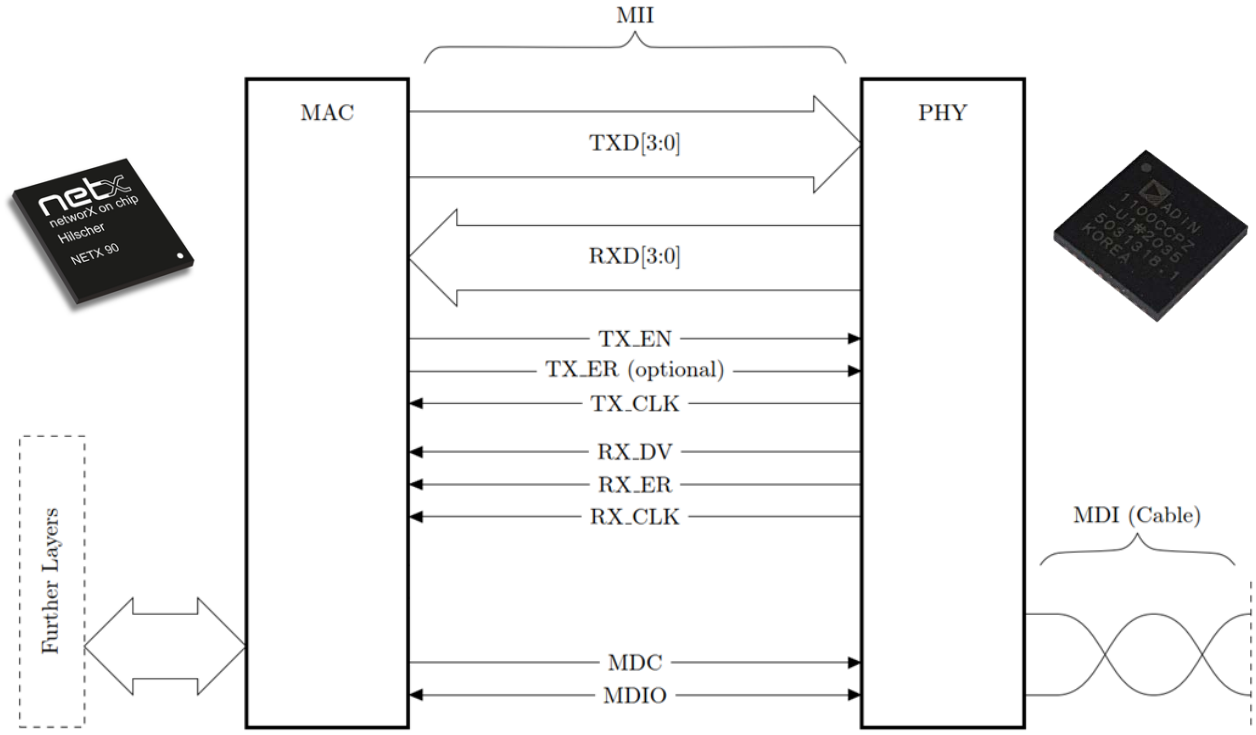

Figure 4: Media Independent Interface, which connects the PHY and the MAC

The interface consists of:

Four data bits (TXD[3:0] and RXD[3:0]) for each data direction (receiving and transmitting)

Control signals to signal transmission status between the PHY and the MAC:

- TX_EN: Asserted while a frame is getting transmitted
- RX_DV: Asserted while a frame is being received
- RX_ER and TX_ER: Asserted when an error occurred during receiving / transmitting
- Receiver and transmitter clocks (RX_CLK and TX_CLK), driven by the PHY

Management interface data (MDIO) and clock (MDC), used for management functions and to configure the PHY from the host microcontroller.

In full configuration the MII uses 16 signal lines. However, the TX_ER signal is optional and not needed in combination with a netX 90. Refer to section *Pin assignment discussion* on page 29 for more information on the pin assignment.

As four bits are transmitted in parallel, the MII is clocked at a quarter of the current link speed, in the case of 10BASE-T1L at 2.5 MHz. This clock is driven by the PHY, so the MAC does not have to be aware of the current link speed on the MDI. It supplies new transmit data on every rising clock cycle. The MDIO interface is part of the MII, but its clock is independent of MII clock. It always clocks at a frequency given by the MAC, which must not be higher than 2.5 MHz, but can be lower if necessary [1].

5.2 MDIO interface

The MDIO interface is implemented by two signals:

- MDIO Interface Clock (MDC): clock driven by the MAC device to the PHY.
- MDIO data: bidirectional, the PHY drives it to provide register data at the end of a read operation.

To configure the PHY from the host microcontroller, the management interface MDIO is used. As a simple bidirectional two-wire interface, it allows the configuration of up to 32 independent PHYs in software during runtime. Status information from the PHYs, such as link status or link speed / mode, can also be obtained via this interface.

As shown in Figure 5, a specific pull-up is used to set the idle state on the data line of the MDIO signal. The clock is supplied from the MAC at a maximum frequency of 2.5 MHz. When reading from a PHY, the MAC stops driving the data line (goes into a high impedance state) and the respective device starts writing the contents of the requested register to the data line.

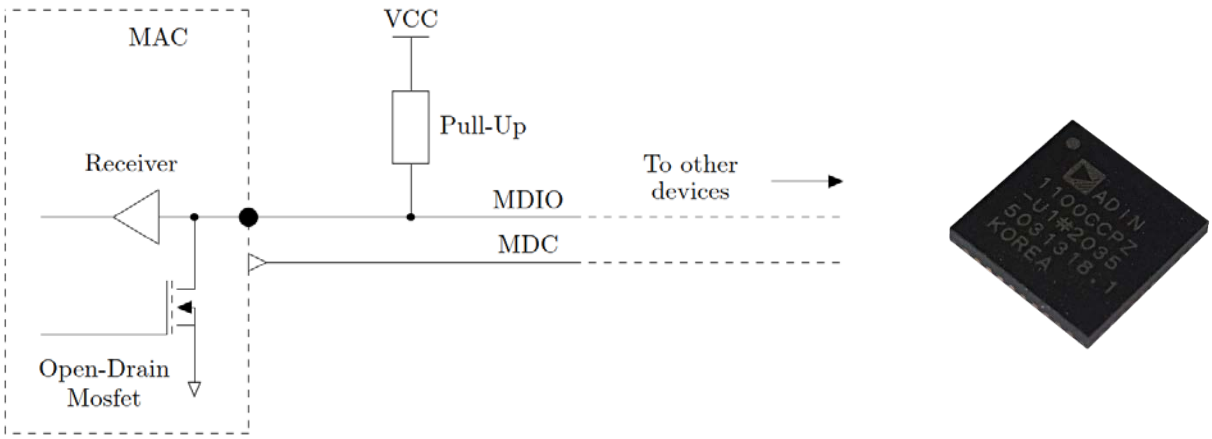

Figure 5: Schematic of the MDIO interface

5.2.1 Communication and clause 22 frame format

To configure the PHY, a set of 32 x 16-bit wide registers is available via MDIO. The MAC can read or write data from or to this set registers using management frames. The IEEE802.3 specification only defines register 0 (control) and 1 (status) as mandatory. Registers above 14 can be assigned by the PHY manufacturer to implement vendor-specific functions [1].

Table 5 shows the frame format for clause 22 management frames. The data is transmitted from left to right.

Operation	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Write to register	1…1	0 1	0 1	X X X X X	X X X X X	1 0	16-bit data	Z…
Read from register	1…1	0 1	1 0	X X X X X	X X X X X	Z 0	16-bit data	Z…

Table 5: MDIO clause 22 frame format

5.2.2 Changes in clause 45

The ADIN1100 PHY does support the updated version of MDIO described in IEEE802.3 clause 45. This version of MDIO changes the way individual registers are addressed without changing the format of the management frames.

As shown in Table 6, the start of frame indicator **ST** changed as well as the possible operations **OP**. Furthermore, DEVAD now describes not a single register, instead it selects a whole bank of registers in the PHY. Each bank is also called an MDIO Manageable Device (MMD). Each subsection of the PHY (e.g. auto-negotiation, PMA, PCS, etc.) may have its own MMD with an individual set of registers. Refer to the datasheet of the PHY for more information.

To select a register to read from to or write to, the *Select register* frame has to be send prior to the read or write frame with the MMD number as well as the register address in the data field of the frame. The PHY then latches this address for further read or write accesses. This system allows a PHY to have a total of 32 MMDs each with $2^{16} = 65536$ individual registers.

Operation	PRE	ST	OP	PHYAD	DEVAD	TA	DATA	IDLE
Select register	1…1	0 0	0 0	X X X X X	X X X X X	1 0	16-bit register address	Z…
Write to register	1…1	0 0	0 0	X X X X X	X X X X X	1 0	16-bit data	Z…
Read from register	1…1	0 0	1 1	X X X X X	X X X X X	Z 0	16-bit data	Z…
Read + increment latched address	1…1	0 0	1 0	X X X X X	X X X X X	Z 0	16-bit data	Z…

Table 6: MDIO clause 45 frame format

6 Hardware design considerations

6.1 SPE front-end

The analog front-end is the circuit between the MDI connector and the PHY. It is used to both isolate the signal as well as to reduce noise and interference that may be present on the MDI.

Another part of the front-end is the termination circuit for the PHY after the isolation, as specified in the datasheet. This circuit is used to reduce the echo to the PHY receiver during transmission. The front-end also incorporates TVS diodes for over-voltage protection which have to be placed near the PHY on the board.

6.1.1 Industrial specifications

To use 10BASE-T1L in an industrial environment, the specification IEC 62368-1 states a minimum isolation voltage of 1500 VAC for 60 seconds [6]. To comply with the specification, NXEB 90-SPE evaluation board uses the front-end design with a signal transformer proposed by Würth which is shown in Figure 6.

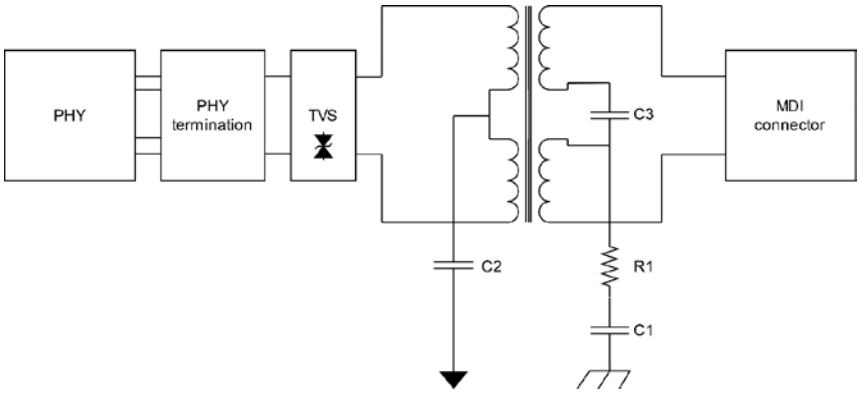

Figure 6: Inductively coupled 10BASE-T1L front-end proposed by Würth

A signal transformer is used to isolate the MDI from the rest of the circuit. Common-mode filtering is done in the transformer, no CMC is needed in 10BASE-T1 applications. R1 and C1 are used as a termination network to chassis ground. In industrial applications, the capacitor C1 needs to withstand 2 kV or more. C2 is used as blocking capacitor to ensure no constant current is flowing to ground. The PHY sends its data signal with an offset respective to the circuit's ground as it cannot generate negative voltages required for the 10BASE-T1L signal on its own. The transformer will then remove this offset, generating the $\pm$1 V or $\pm$2.4 V signal.

C3 improves the low-frequency performance in 10BASE-T1 applications. When using a transformer without a split center tap, this capacitor may also be swapped with two caps in series with the MDI lines. The following component values were chosen for this design based on Würth's recommendations [6]:

1. **C1:** 1 nF 2000 V, 1206 in size
2. **C2:** 100 nF 50 V, 0603 in size
3. **C3:** 470 nF 50 V, 1210 in size
4. **R1:** 100 Ω 1%, 0805 in size

The whole analog front-end circuit, combined with a TVS diode and the mixing circuit as stated in the ADIN1100 datasheet is shown in Figure 7.

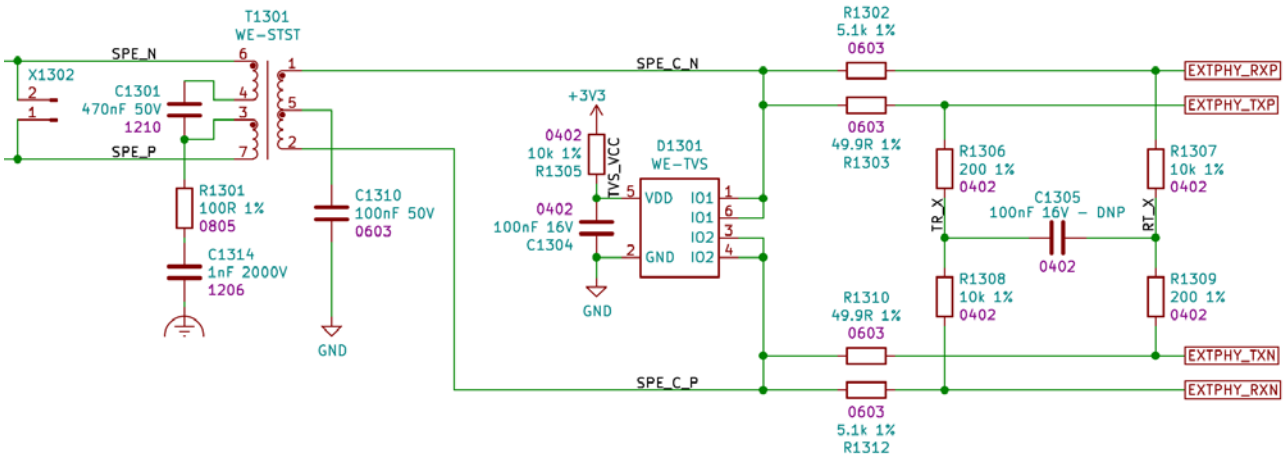

Figure 7: Analog front-end with signal transformer to be used with ADIN1100 external PHY

6.2 ADIN1100 hardware configuration

6.2.1 Bootstrapping

The ADIN1100 features some options that can be configured in hardware using pull resistors on specified pins. This configuration is latched after the reset phase of the PHY and the pins continue with their normal function.

The following features listed in this section should be set in hardware. The rest of the configuration is done via MDIO during runtime.

6.2.1.1 MII mode

Besides normal MII operation, the ADIN1100 supports RMII and RGMII too. The desired normal MII mode can be selected in hardware with the configuration listed in Table 7.

PHY pin	Pull resistor required?
RX_ER / MACIF_SEL1	Pull up to PHY VDDIO with 4.7 kOhm
RX_CLK / RXC / MACIF_SEL0	Pull up to PHY VDDIO with 4.7 kOhm

Table 7: ADIN1100 MII mode configuration

6.2.1.2 Software power-down

When the board is powered, the PHY has to remain in a power-down state until initialized via MDIO. To select *Software power-down after reset*, configure the pins as listed in Table 8.

PHY pin	Pull resistor required?
RX_DV / RX_CTL / SWPD_ENB	No pull-up required (internally pulled down)

Table 8: ADIN1100 “Software power-down after reset” configuration

6.2.1.3 MDIO address

To configure the hardware address of the PHY for MDIO communication, the ADIN1100 has three configurable bits. Table 9 shows the recommended address configuration depending on the xC channel it is connected to.

PHY pin	Pull resistor required?
LINK_ST / PHYAD_2	No pull-up required (internally pulled down)
RXD_3 / PHYAD_1	No pull-up required (internally pulled down)
RXD_2 / PHYAD_0	PHY on xC channel 0: No pull-up required (internally pulled down) PHY on xC channel 1: Pull-up to PHY VDDIO with 4.7 kOhm

Table 9: ADIN1100 MDIO address configuration

6.2.2 External interrupt

When the ADIN1100 signals an event (link status change, auto-negotiation change, etc.), the interrupt pin is pulled low. Being an open collector output, it needs to be pulled up to VDDIO to set its idle state as shown in Figure 8.

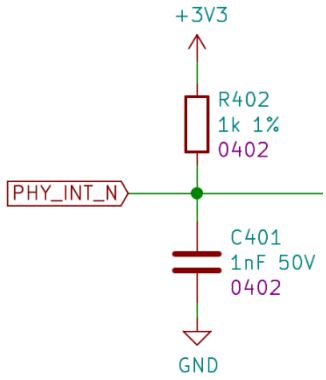

Figure 8: External interrupt

It is also recommended to decouple this pin with a small capacitor to reduce interference that may be induced. A pull-up of 1 kOhm and a 1 nF capacitor to ground are used on the NXEB 90-SPE evaluation board.

Refer to section *External PHY* control on page 31 for pin assignment information.

6.2.3 Clocking

The ADIN1100 requires either a crystal oscillator with a frequency of 25 MHz ±30 ppm [5], or an external clock input. Depending on the setup used, a different hardware schematic is needed.

Figure 9 shows the variant implemented on the NXEB 90-SPE: External clock. The figure shows the assembly option with a 25 MHz crystal.

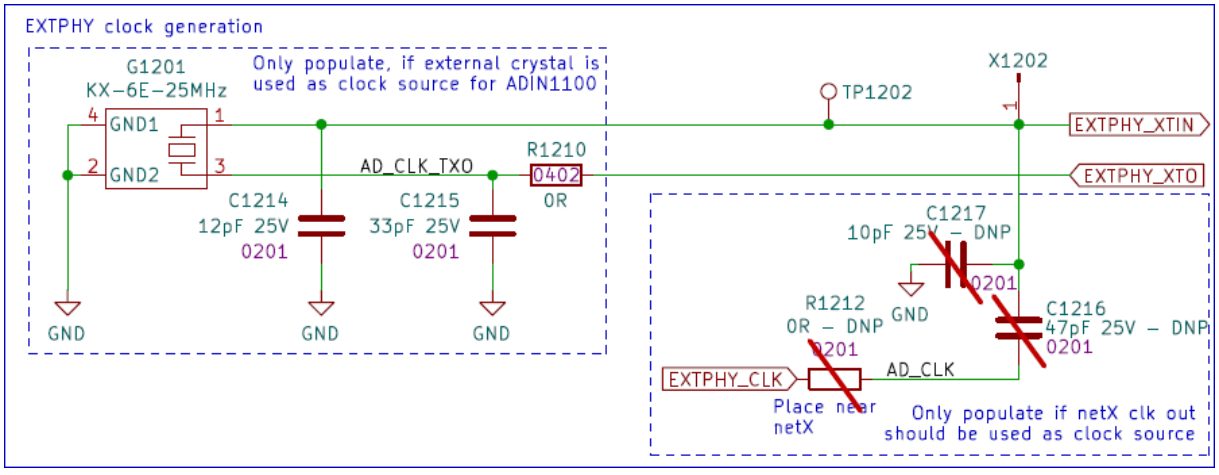

Figure 9: Possible clock setups for the ADIN1100

When using the netX 90 CLK25OUT pin, a capacitor divider network is needed as the ADIN1100 expects a maximum of 2.4 V pk-pk at its clock input. For more information, refer to the datasheet of the ADIN1100.

6.3 Link and activity LEDs

The netX 90 MLED units 2 and 3 are used by default to connect to a dual LED for link and activity for each xC port. These units will generate the blinking activity LED based on the MII signals of the respective port. Figure 10 shows the schematic (on the left).

To drive the dual LEDs correctly, the power circuit shown in Figure 10 on the right is needed. The schematic is part of reference [10].

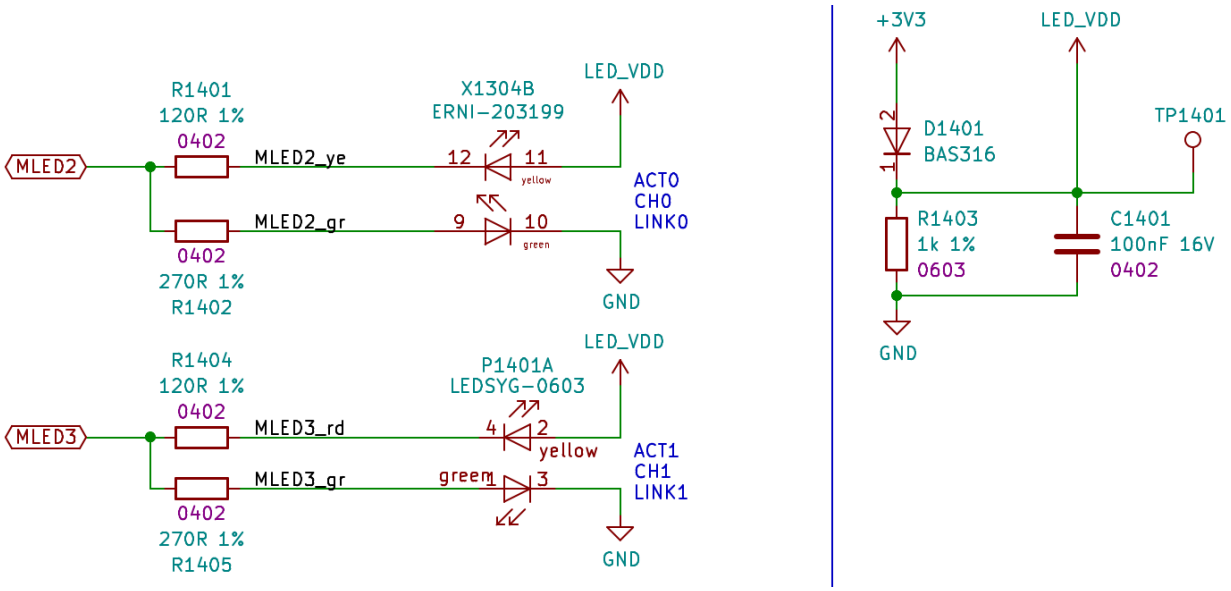

Figure 10: Left: MLEDs for link and activity on both ports – Right: Power circuit for all MLEDss

6.4 Power measurements and discussion

6.4.1 Power measurements

For a SoC such as the netX 90 with interconnected external components like SDRAM, Flash, and a 10SPE PHY supplied by 3.3 V DC, it is common to differentiate between peak and average current, particularly in the context of power management and design:

- **Peak current:** Refers to when multiple components (e.g. SoC, SDRAM, Flash, 10SPE PHY) are active simultaneously, such as during processing bursts or boot-up. The DC/DC converter, supported by capacitors in the design, must handle these peaks to avoid voltage dips.
- **Average current:** Represents the steady-state current drawn by the SoC and peripherals. With external SDRAM and Flash, the average current is higher than for standalone operation, so optimizing the converter for this load ensures efficient, stable power delivery.

In DC power contexts, average current provides a baseline for sizing the power supply, while peak current helps in handling transient loads due to simultaneous activity across external peripherals. In the following chapter, all measurements refer to average current.

10SPE PROFINET IO-Device reset test condition (Board held in reset)

The test uses NXEB 90-SPE revision 4 (room temperature)

Connector		**Board in reset**		
Ref	**Description**	**I (mA)**	**U (V)**	**P (mW)**
JP202	netX 90 total power consumption measurement header	~ 42	3.285	~ 137.97
JP204	1.2 V output netX 90 (on-chip DC/DC converter)	55	1.267	69.69
JP203	1.2 V supply netX 90 for internal PHYs (power down)	0	1.227	0
JP205	3.3 V supply netX 90 for internal PHYs (power down)	10	3.316	33.16
JP1201	3.3 V supply for ADIN1100 (external 10BASE-T1L)	~ 2	3.317	~ 6.6
JP702	3.3 V supply of the whole board	~ 67	3.33	~ 223.11

Table 10: Power measurements: 10SPE PROFINET IO-Device reset test condition (Board held in reset)

10SPE PROFINET IO-Device measurement condition 1 (netX 90 APP is disabled)

The following measurement conditions apply:

- NXEB 90-SPE revision 4 (room temperature)
- Companion chip solution (Application CPU is disabled, SPM is enabled)
- Integrated on-chip dual 10BASE-T/100BASE-TX PHY in power-down mode
- Use case C Single-Port SPE PROFINET IO-Device LFW V5.6.2.0 (PHY address = 3) with SPE support
- Configuration with 256 bytes input / 256 bytes output
- Established active network connection for cyclic data exchanges with a controller (1 ms network cycle time)

Connector		**Board is running (Communication with controller)**		
Ref	**Description**	**I (mA)**	**U (V)**	**P (mW)**
JP202	netX 90 total power consumption measurement header	65.9 ~ 66.1	3.327	~ 219.91
JP204	1.2V output netX 90 (on-chip DC/DC converter)	93.7 ~ 94	1.23	~ 115.62
JP203	1.2V supply netX 90 for internal PHYs (power down)	0.0487	1.228	0.06
JP205	3.3V supply netX 90 for internal PHYs (power down)	10.42	3.327	34.67
JP1201	3.3V supply for ADIN1100 (external 10BASE-T1L)	33.84 ~ 34.92	3.328	~ 112.89
JP702	3.3V supply of the whole board	135.7 ~ 135.9	3.33	~452.55

Table 11: Power measurements: 10SPE PROFINET IO-Device measurement condition 1 (netX 90 APP is disabled)

10SPE PROFINET IO-Device measurement condition 2 (netX 90 APP is enabled)

The following test conditions apply:

- NXEB 90-SPE revision 4 (room temperature)
- Stand-alone chip solution (Application CPU is enabled, internal DPM is enabled)
- Integrated on-chip dual 10BASE-T/100BASE-TX PHY in power-down mode
- External 10BASE-T1L PHY with single 3.3 V supply in 2.4 Vp-p transmit level mode
- Use case C Single-Port 10SPE PROFINET IO-Device LFW V5.6.2.0 (PHY address = 3) with SPE support
- Host example for NXEB 90-SPE device: NXSLFWPNSV5_V4.1.0.1_SPE_1-Port: 6 bytes input / 10 bytes output
- Established active network connection for cyclic data exchanges with a controller (1 ms network cycle time)

Connector		**Board is running (Communication with controller)**		
Ref	**Description**	**I (mA)**	**U (V)**	**P (mW)**
JP202	netX 90 total power consumption measurement header	72.8 ~ 73.2	3.327	~ 243.54
JP204	1.2V output netX 90 (on-chip DC/DC converter)	100.7 ~ 101.1	1.23	~ 124.353
JP203	1.2V supply netX 90 for internal PHYs (power down)	0.0525	1.228	0.064
JP205	3.3V supply netX 90 for internal PHYs (power down)	10.26	3.327	34.135
JP1201	3.3V supply for ADIN1100 (external 10BASE-T1L)	33.84 ~ 33.92	3.328	~ 112.89
JP702	3.3V supply of the whole board	142.2 ~ 145.7	3.33	~485.18

Table 12: Power measurements: 10SPE PROFINET IO-Device measurement condition 2 (netX 90 APP is enabled)

6.4.2 Board measurement discussion

The netX Studio CDT project examples, including all firmware components and configuration files, which were used to measure the average current consumption, are provided as part of the release package for the NXEB 90-SPE evaluation board. Reference:
https://hilscher.atlassian.net/wiki/x/kVCYC
The NXEB 90-SPE evaluation board is equipped with the netX 90, interconnected with a 10BASE-T1L PHY (MII at 25 MHz), 8 MByte SDRAM (16-bit at 100 MHz), and 4 MByte serial NOR Flash (4-bit at 80 MHz).

Firmware use case C refers to a fully featured, loadable communication firmware with extended webserver capabilities that requires external SDRAM and serial NOR Flash, together with a Flash file system. The Flash layout, along with detailed information on firmware images, is explained and shown in the netX 90 Production Guide, reference:
https://hilscher.atlassian.net/wiki/x/JyOiB

The average current consumption measured above reflects steady-state firmware operation during active cyclic data exchanges over the network with a controller, indicating a high utilization rate for the 10BASE-T1L PHY and a low utilization rate for the 8 MByte SDRAM and 4 MByte serial NOR Flash. In principle, the SDRAM utilization rate is higher when file operations are performed, as the management structures of the file system reside in the SDRAM. Furthermore, the serial NOR Flash utilization rate is higher during the boot sequence, the streaming of webserver content, and the firmware update procedure.

Note: In general, firmware use case C (as in this case without IoT capabilities such as OPC UA or MQTT) is likely to have a low to medium SDRAM utilization rate. In case the SDRAM controller operates in split mode (dividing the memory resources equally between the communication side and the application side), the SDRAM is likely to have a medium to high utilization rate, depending on the use case and application software.

16-bit SDRAM

The IS45S16400J is a 64 Mb (4M x 16) synchronous DRAM (SDRAM), with the following maximum current parameters (7BLA2) defined in the datasheet, reference:
https://www.issi.com/WW/pdf/42-45S16400J.pdf

Current parameters (3.3 V supply):

- Operating current: 70 mA (when actively reading/writing one bank)
- Standby current: 20 mA (when idle but not in deep sleep)
- Auto-refresh current: 90 mA (during refresh of all banks)
- Self-refresh current: 2 mA (in deep sleep mode)

In the active phase, the operating current could reach 70 mA when a single bank is accessed continuously at high speed.

The total average current for the entire SDRAM will be lower in practice because the memory is not operated at full clock speed (100 MHz instead of 133 MHz) and is not accessed continuously, leading to a lower overall utilization rate:

- At low utilization (idle with occasional access): Current consumption derives primarily from standby or self-refresh modes, resulting in low power usage
- At medium utilization (alternating between active and idle): Current consumption is a blend of active and refresh modes, resulting in moderate power usage.
- At high utilization (active with constant access): Current consumption is driven primarily by the active mode, resulting in high power usage

Note: The IS42S16400J-7BLA2 is no longer recommended for new designs, reference https://hilscher.atlassian.net/wiki/x/0VOYC
A suitable alternative is the AS4C4M16SA-7BAN, with a lower maximum refresh current of 55 mA and a maximum operating current in burst mode (multi-bank interleave) of 70 mA. The average current consumption measured in the section above reveals a low utilization rate.

4-bit serial NOR Flash

The MX25L3233F is a 32 Mb serial NOR Flash memory device, with the following maximum current parameters defined in the datasheet, reference:
https://www.macronix.com/Lists/Datasheet/Attachments/8933/MX25L3233F, 3V, 32Mb, v1.7.pdf

Current parameters (3.3 V supply):

- Read current: 17 mA (during active reading)
- Program current: 15 mA (during active writing)
- Erase current: 15 mA (during active sector erasing)
- Standby current: 50 µA (not actively reading, writing, or erasing)

While the read current at 80 MHz clock speed will be slightly lower than at 133 MHz, the MX25L3233F datasheet provides a separate current specification for 50 MHz only.

The total average current for the entire serial NOR Flash will be lower in practice because the memory is not accessed continuously, leading to a lower overall utilization rate:

- At low utilization: Mostly idle with very few operations, leading to lower power consumption from standby mode.
- At medium utilization: Moderate usage with a balanced mix of read, write, and idle periods, leading to moderate power consumption.
- At high utilization: Frequent read and write operations with minimal idle time, resulting in high active power consumption.

Note: The average current consumption measured in the section above reveals a low utilization rate.

Single-Pair Ethernet PHY

The ADIN1100 is a 10BASE-T1L Single-Pair Ethernet PHY, with the following typical current parameters defined in the datasheet, reference:
https://www.analog.com/media/en/technical-documentation/data-sheets/adin1100.pdf

Active current (single 3.3 V supply):

- 1.0 V p-p Mode: 25 mA (during active data transmission with 1.0 V peak-to-peak output).
- 2.4 V p-p Mode: 33 mA (during active data transmission with 2.4 V peak-to-peak output, requiring higher current for greater signal amplitude).

The 10BASE-T1L PHY supports two transmission modes according to IEEE 802.3cg for standard industrial use and intrinsically safe application designs. In general, with cyclic data exchanges, automation applications account for high utilization rates.

Note: The ADIN 1100 datasheet provides typical current parameters and not maximum current parameters. The average current consumption measured in the section above reveals a high utilization rate. The measured current in 1.0 V p-p mode was 27.6 mA.

netX 90 Multiprotocol SoC

The conditions outlined in the manual for the overall current consumption of the netX 90, including digital, analog, PHY, and I/O, derive from a high utilization rate, reference:
https://hilscher.atlassian.net/wiki/x/ICOiB
The netX 90 requires a single 3.3 V external voltage supply, due to the integrated step-down converter with external LC circuitry for the 1.2 V core voltage, with the following current parameters (for comparison at room temperature):

- 3.3 V supply current I/O domain without PHY: 130 mA (high utilization rate)
  - 3.3 V supply current I/O dual Ethernet PHY: 80 mA (during active operation)
  - 3.3 V supply current I/O dual Ethernet PHY: 11 mA (in power done mode)
- DC/DC 1.2 V supply current I/O domain without PHY: 155 mA (high utilization rate)
  - DC/DC 1.2 V supply current I/O dual Ethernet PHY: 55 mA (during active operation)
  - DC/DC 1.2 V supply current I/O dual Ethernet PHY: 53 µA (in power done mode)

External 3.3 V single supply:

3.3 V supply current I/O domain with PHY (in power-down mode): 141 mA

Note: The average current consumption measured in the section above for the 3.3 V supply reveals a modest utilization rate for the netX 90, largely because the on-chip Ethernet PHY is in power-down mode and that one active xC channel is required for the single-port communication firmware, coupled with a low utilization rate for the external memory and a simple I/O config application.

Step-Down Converter

The input current of the integrated DC/DC converter is lower than the output current due to the principle of power conservation. The principle operation consists of two phases: the initial switching-on phase and the steady-state operation phase:

- Inrush current: When a DC/DC converter is first powered on, it experiences an inrush current. This is the initial surge of current as the capacitor charges and the inductor begins to store energy.
- Steady-state current: Once the converter reaches its steady-state operation, the current stabilizes depending on the load, which the converter is designed to handle efficiently over long periods.

The load and the efficiency of the converter determine the steady-state operation:

$$\eta = P_{out} / P_{in} = (V_{out} \times I_{out}) / (V_{in} \times I_{in}) \text{ with } P_{loss} = P_{in} - P_{out}$$

where P_{out} is the output power, P_{in} is the input power, and η is the efficiency of the converter.

Example: If the load is 100 mA (see measurements above) and the efficiency of the converter is 0.95 (see simulation below, with parasitic adjustments), the input current, drawn from the netX 90 3.3 V supply, will be around:

$$I_{in} = (1.2 \text{ V} \times 100 \text{ mA}) / (3.3 \text{ V} \times 0.95) = 38.3 \text{ mA}$$

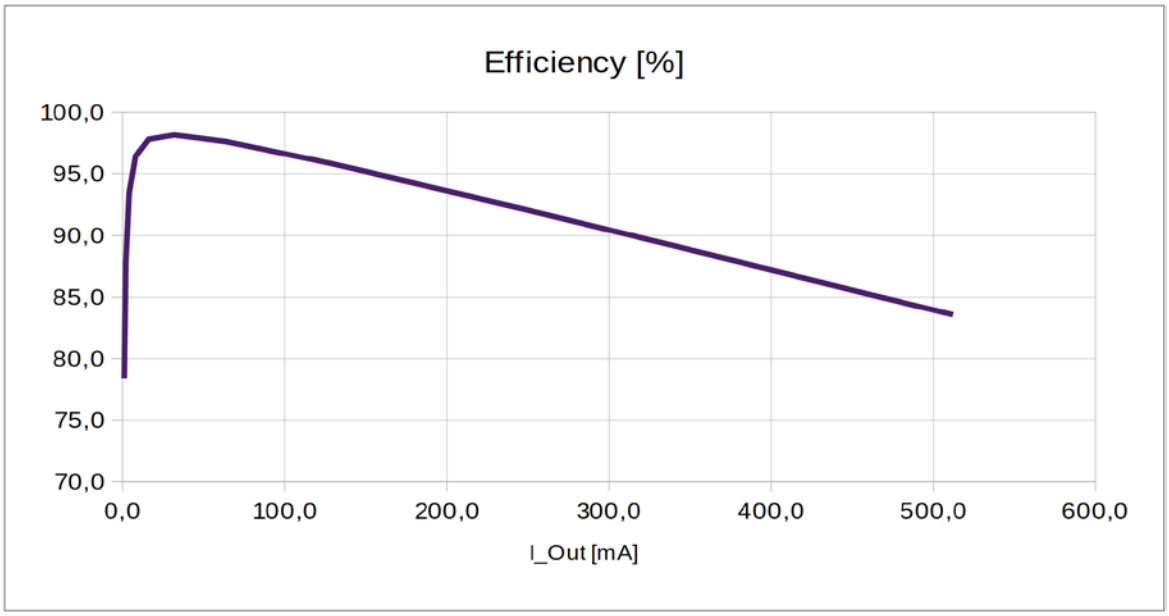

Figure 11: DC/DC efficiency (simulation results using ideal external components)

The DC/DC converter has built-in slew rate control to limit the inrush current by controlling the rate of the voltage rise (soft start-up ramp):

$$I_{inrush} = C \times dV / dt$$

where C is the total capacitance and dV/dt is the rate of the input voltage change.

Example: If the capacitance is 11 µF and the input voltage ramps up with 4.5 V/ms (max), the inrush current, drawn from the netX 90 3.3 V supply, will be around:

$$I_{inrush} = 11 \text{ µF} \times 4.5 \text{ V/ms} = 49.5 \text{ mA}$$

Note: The soft start-up ramp ensures that the digital core starts after the ramp reaches 99% of the core voltage, assuming the core is not held in reset, e.g.
(0.99 × 1.2 V) / 4.5 V/ms = 264 µs.

Current Consumption Impact

The 3.3 V power supply should be designed to support peak current levels with safety margins, ensuring reliable performance without drops in voltage stability during load transitions. Peak currents are calculated by accounting for various components, which often do not peak simultaneously, allowing for a more distinct analysis:

- List the peak currents
- Determine usage patterns
- Estimate non-simultaneous peaks
- Add a safety margin

For instance, the external serial NOR Flash holds a file system, including a webserver, for configuration purposes and firmware updates that require higher usage of external SDRAM, but where the actual application usually enters a configuration or maintenance cycle.

Component	Peak Current (mA)	Comment
netX 90	To be measured	Account for thermal effects
ADIN1100	To be measured	Account for thermal effects
AS4C4M16SA	70.0	Maximum operating current (burst mode)
MX25L3233F	17.0	Maximum operating current (continues read)

Note: The netX 90 current consumption for the 3.3 V supply varies significantly by application, affecting CPU load, memory footprint, peripheral usage, and I/O pin activity, which is influenced by device configurations, software scenarios, use cases, utilization rates, and operating temperatures. The NXEB 90-SPE evaluation board provides various current measurement test headers for the netX 90 and the ADIN1100, allowing, for instance, the use of a power analyzer to measure both peak and average current consumption.

Power supply recommendations:

- Power supply 3.3 V: Ensure the supply delivers peak performance with safety margins to account for transients and peaks
- Capacitors: Use decoupling capacitors to manage voltage fluctuations and add bulk capacitors to handle longer transients
- Voltage stability: Ensure good voltage regulation with low ripple to avoid instability between low and high current activities

Single Pair Power over Ethernet (SPoE):

- The ADIN1100 PHY vendor offers reference designs for a suitable Industrial SPoE PD Controller (e.g. LTC9111)

7 Use case for SPE

The netX 90 can use its two flexible communication (xC) channels to implement either up to two independent IEEE802.3 Ethernet MACs or a 2-port switch with integrated MAC.

Each xC channel has its own MII interface, which is connected by default to one port of the internal PHY for 10BASE-T / 100BASE-TX Ethernet. The MII of the xC channels can also independently be multiplexed to the external pins of the netX 90 to be connected to external PHYs.

7.1 Single-port SPE

This variant uses xC channel 1 to connect via the external MII to an ADIN1100 10BASE-T1L PHY as shown in Figure 12. The MII Management Unit (MIIMU), which is used to send and receive MDIO data, of xC channel 1 is furthermore connected to the external MDIO interface and to the PHY to allow it to be configured via software. By default, the MDIO address of the PHY should be set to the same as the xC port number it is connected to.

xC channel 0 will stay in its initial configuration connected to the internal PHY which will is configured in a power-down state in this use case. This frees the external pins on the netX 90 normally associated with external MII0 for other functions.

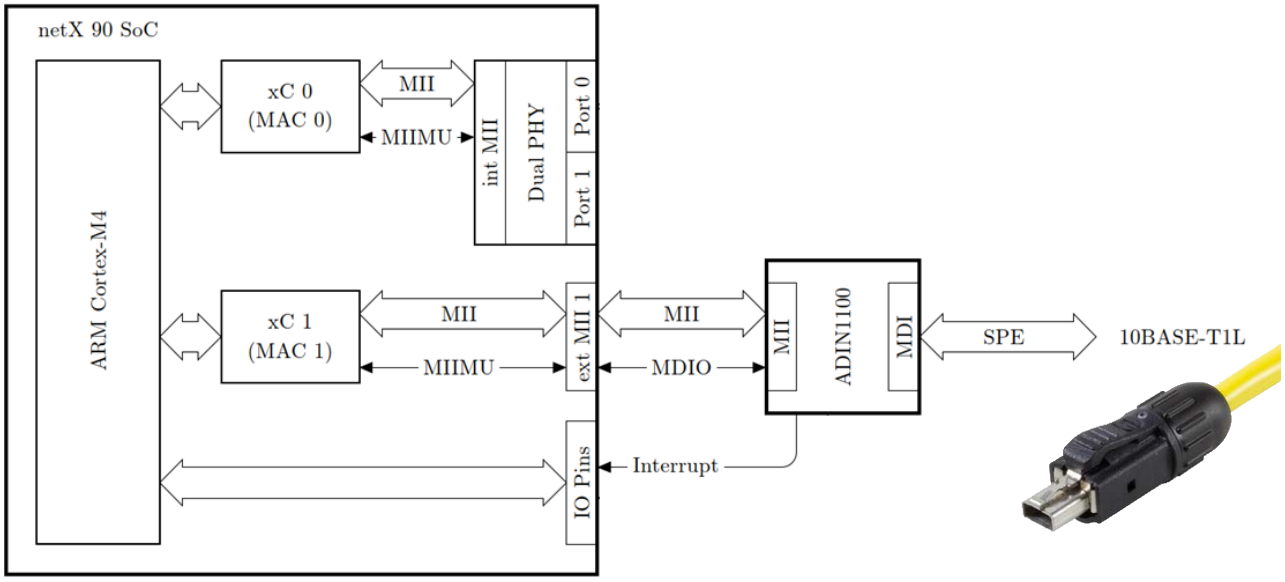

Figure 12: Single port SPE use-case block diagram

The interrupt pin of the external PHY has to be connected to an interruptible pin that is accessible from the COM CPU of netX 90. The link status will be obtained via MDIO when an interrupt is asserted from the PHY.

In this configuration 8 + 9 MMIO pins stay available for single chip designs. For companion chip use cases the serial DPM0 interface is available both in SPI or SQI mode. This use case also allows the use of an external 16-bit SDRAM as well as an external SQI Flash to extend the available memory of the netX 90.

For further information on which pins to use, see section *Pin assignment* discussion on page 29.

7.2 Pin assignment discussion

As the physical pins of the netX 90 are limited, some pins share different functions that can be selected with multiplexing options in software. As this affects the hardware layout, some planning needs to be done up front.

7.2.1 External MII in combination with SDRAM

By default, both external MII interfaces are dedicated their own pins, but some of those pins share their functionality with external SDRAM. To use an external SDRAM in combination with up to two external PHYs, a secondary pin assignment option is used.

This moves some pins of both external MII interface to a different physical location to free up all needed pins for SDRAM. Table 13 lists the pins used for external MII0 and external MII1 with the pin assignment option active. The signals that were moved to a different physical location are marked.

Pad	Pin name	Function
H4	MII0_RXD3	RXD[3:0] of MII0
H5	MII0_RXD2	
J4	MII0_RXD1	
J5	MII0_RXD0	
G4	MII0_RXDV	RX_DV of MII0
F3	MII0_RXER	RX_ER of MII0
F4	MII0_RXCLK	RX_CLK of MII0
H6	MII0_TXD3	TXD[3:0] of MII0
H7	MII0_TXD2	
J6	MII0_TXD1	
J7	MII0_TXD0	
G5	MII0_TXCLK	TX_CLK of MII0
C6	HIF_D13	TX_EN of MII0
B6	HIF_D14	COL of MII0
A6	HIF_D15	CRS of MII0
F8	MII1_RXD3	RXD[3:0] of MII1
F9	MII1_RXD2	
G8	MII1_RXD1	
G9	MII1_RXD0	
F10	MII1_RXDV	RX_DV of MII1
K7	COM_IO0	RX_ER of MII1
D9	MII1_RXCLK	RX_CLK of MII1
H8	MII1_TXD3	TXD[3:0] of MII1
H9	MII1_TXD2	
J8	MII1_TXD1	
J9	MII1_TXD0	
H10	MII1_TXCLK	TX_CLK of MII1
K9	MII1_TXEN	TX_EN of MII1
E2	HIF_RDN	COL of MII1
K6	COM_IO1	CRS of MII1

Table 13: External MII pin assignment with secondary pin assignment option

Note: Even though the COL / CRS pins of both external MIIs are not needed in full-duplex mode, they **must not** be used in PIO mode! The respective xC channel expects them to not be asserted during runtime when in full-duplex mode. The inputs of those pins must be tied to ground in the hardware design. Leaving these pins floating will cause collision errors in the MAC during transmit.

7.2.2 External PHY control

To control the external PHY of the netX 90, the signals listed in Table 14 are used.

The interrupt pins of all connected ADIN1100 external PHYs are combined and connected to the HIF_DIRQ pin. This pin can generate low level interrupts to the COM CPU to tell the software as soon as a link status change on either of the PHYs occurred. The software running on the COM CPU will then access each PHY's interrupt status register via the MDIO interface to determine the source of the interrupt and act accordingly.

The reset output of the netX 90 is used to perform a hardware reset of the ADIN1100 during the initialization phase. Thus, it must be directly connected to the reset input of the PHY and it is important that the PHY is configured via mode pin in software power-down mode after reset. This is to ensure that the PHY does not start establishing a connection until the software of the netX 90 is started to release the PHY from reset.

Pad	Pin name	Function
L9	CLK25OUT	25 MHz clock output
L3	RST_OUT_N	Reset output
F2	HIF_DIRQ	Interrupt input
L8	MII_MDIO	MDIO data
K8	MII_MDC	MDIO clock

Table 14: Control signals for the external PHY from the netX 90

Note: CLK25OUT can be used to substitute the external PHY's oscillator. The frequency accuracy and jitter of this output will depend on the oscillator used for the netX 90. For more information on the hardware schematic, refer to section *Clocking* on page 17.

7.2.3 Serial DPM0 interface and MMIO

Depending on the use case, the DPM0 interface is either available in SQI or SPI mode. This also limits the amount of MMIO pins that are available to the application processor in the netX 90. This section lists the pin assignment for these interfaces.

Single-Port SPE use case

The Single-Port SPE use case supports the serial DPM0 interface either in SPI or SQI mode. Table 15 lists the signals used for serial DPM0 in SQI mode.

Pad	Pin name	Function
B8	HIF_D8	DPM0_SQI_SIO1
A8	HIF_D9	DPM0_SQI_SIO0
C7	HIF_D10	DPM0_SQI_CSN
B7	HIF_D11	DPM0_SQI_CLK
A7	HIF_D12	DPM0_SQI_DIRQ
C6	HIF_D13	DPM0_SQI_SIRQ
B6	HIF_D14	DPM0_SQI_SIO2
A6	HIF_D15	DPM0_SQI_SIO3

Table 15: Signals for serial DPM0 in SQI mode

For SPI mode, Table 16 lists the signals used for the serial DPM0 interface in SPI mode.

Pad	Pin name	Function
B8	HIF_D8	DPM0_SPI_MISO
A8	HIF_D9	DPM0_SPI_MOSI
C7	HIF_D10	DPM0_SPI_CSN
B7	HIF_D11	DPM0_SPI_CLK
A7	HIF_D12	DPM0_SPI_DIRQ

Table 16: Signals for serial DPM0 in SPI mode only

Table 17 lists the available MMIO pins in case of using only one external PHY. The pins marked in orange are not available in case the netX 90 is used as a companion chip with serial DPM0 in SPI mode. The pins marked in blue are furthermore not available when using SQI mode for this interface, but can be used in SPI mode.

Pad	Pin name	Function
M7	MMIO0	Multiplex matrix IO 0
L7	MMIO1	Multiplex matrix IO 1
M6	MMIO2	Multiplex matrix IO 2
L6	MMIO3	Multiplex matrix IO 3
M5	MMIO4	Multiplex matrix IO 4
L5	MMIO5	Multiplex matrix IO 5
M4	MMIO6	Multiplex matrix IO 6
L4	MMIO7	Multiplex matrix IO 7
B8	HIF_D8	Multiplex matrix IO 8
A8	HIF_D9	Multiplex matrix IO 9
C7	HIF_D10	Multiplex matrix IO 10
B7	HIF_D11	Multiplex matrix IO 11
A7	HIF_D12	Multiplex matrix IO 12
C6	HIF_D13	Multiplex matrix IO 13
B6	HIF_D14	Multiplex matrix IO 14
A6	HIF_D15	Multiplex matrix IO 15

Table 17: MMIOs available with one external PHY

8 Appendix

8.1 List of tables

8.2 List of figures

8.3 Legal notes

Copyright

Important notes

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The warranty obligation shall not apply if the notification of defect is not asserted promptly, if the purchaser or third party has tampered with the products, if the defect is the result of natural wear, was caused by unfavorable operating conditions or is due to violations against our operating regulations or against rules of good electrical engineering practice, or if our request to return the defective object is not promptly complied with.

Costs of support, maintenance, customization and product care

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The customer must not use this confidential information to his own advantage or for his own purposes or rather to the advantage or for the purpose of a third party, nor must it be used for commercial purposes and this confidential information must only be used to the extent provided for in this agreement or otherwise to the extent as expressly authorized by the disclosing party in written form. The customer has the right, subject to the obligation to confidentiality, to disclose the terms and conditions of this agreement directly to his legal and financial consultants as would be required for the customer's normal business operation.

Export provisions

The delivered product (including technical data) is subject to the legal export and/or import laws as well as any associated regulations of various countries, especially such laws applicable in Germany and in the United States. The products / hardware / software must not be exported into such countries for which export is prohibited under US American export control laws and its supplementary provisions. You hereby agree to strictly follow the regulations and to yourself be responsible for observing them. You are hereby made aware that you may be required to obtain governmental approval to export, reexport or import the product.

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