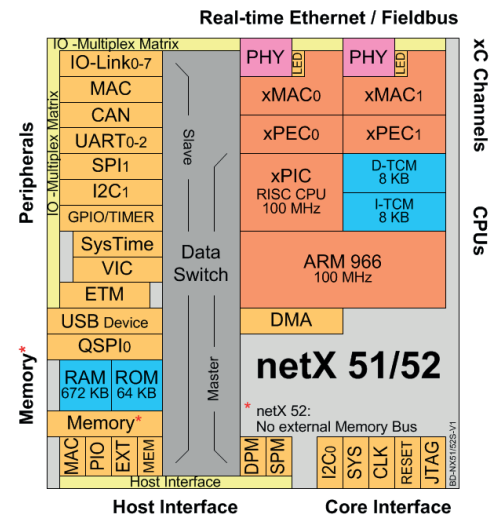


# netX 51

More functions & higher Performance  
for Real-Time Ethernet

- Two communication channels for Real-Time Ethernet equipped with PHY or fieldbus
- Extended communication function support amongst others, PROFINET V2.3 - Dynamic Frame Packing and IO link V1.1
- Second RISC CPU for time-critical IO tasks
- Additional CAN and MAC controller
- Fast SPI host interface with Read/Write functions



## Flexible „high end“ network controller equipped with a host interface or stand-alone solution for digital I/Os

Real-Time Ethernet systems are successfully used and further developed in many applications. The demands made on the resources and functionalities of network controllers are therefore increasing. The network controllers netX 51/52 bank on the further developed netX 50 communications architecture, which features considerably more internal storage capacity and additional function units. The netX 51 hardware is compatible with the netX 50. The netX 52 contains the same silicon, but dispenses with an external memory bus, and due to its smaller housing, is more cost-effective.

These three components are thus optimized for designing modular or compact slaves, or as a Real-Time Ethernet controller on a high-performing CPU. The communication channels take all actual and future requirements from the PROFINET Specification V2.3, such as „Dynamic Frame Packing,“ into consideration. Furthermore, the new PHYs manufactured by Renesas are applied, ensuring faster throughput times and expanded diagnosis properties. Through the internal memory for more than 670 KByte, it is possible to build together with a QSPI Flash very compact solutions with twice the performance of netX 50.

For processing the fast IOs, the application is provided with a second RISC CPU. It works in parallel to ARM and significantly relieves the demands made on the ARM software via short bus cycle times. Typical applications are IO-Link Master Gateways. The xPIC takes over the IO-Link data transfer, leaving the ARM completely available for processing the transmission protocol to the master. A third Ethernet interface for connecting a PC for diagnosis and configuration purposes is implemented. Alternatively, it can also be used for connecting the netX to a host CPU. The netX then behaves like a PHY on this MII interface.

Some Real-Time Ethernet systems use the CANopen object models or the same communication services such as EtherNet/IP and DeviceNet. This results in the task of connecting CAN as the „legacy“ network to the Real-Time Ethernet system. Up to now, that entailed using an expensive netX 100 controller, with its three communication channels. As an alternative, a dedicated CAN controller is now available. With this possibility, the netX 51/52 is so much more than just a Real-Time Ethernet interface chip equipped with a dual-port memory.



→ QR Code Link: netX 51  
Service-Hotline: +49 (0) 6190 9907-90  
[www.hilscher.com](http://www.hilscher.com)

# Product information

## Technical Data

Technical Data	
<b>Processor</b>	ARM 966E-S, 100 MIPS, ARMv5TE instruction set with DSP extension, timer, interrupt and DMA controller xPIC, 32-bit RISC, 100 MIPS, TCM: 8 KByte data, 8 KByte commands
<b>RAM</b>	672 KByte
<b>ROM</b>	64 KByte with bootloader
<b>Ports</b>	2 × 10BASE-T / 100BASE-TX, half/ full duplex, IEEE 1588 time stamp
<b>PHY</b>	Integrated, auto-negotiation, auto-crossover
<b>Real-Time Ethernet</b>	EtherCAT with eight FMMUs and eight sync managers, EtherNet/IP, Modbus IDA, POWERLINK with integrated hub, PROFINET RT and IRT with integrated switch, according to PROFINET V2.3, SERCOS, VARAN
<b>Fieldbus</b>	The systems can be freely combined. AS-Interface (Master), CANopen (Master and Slave), CC-Link (Slave), DeviceNet (Slave), PROFIBUS (Slave)
<b>IO-Link Controller</b>	8 channels, data link layer control via xPIC, IO-Link V1.1
<b>MII-Interface</b>	Configurable in PHY or MAC mode, DMA support for Ethernet frames, HAL API operates with xPIC
<b>CAN Controller</b>	SJA1000 compatible
<b>IEEE 1588 system time</b>	32-bit second counter, 32-bit nanosecond counter
<b>USB</b>	Revision 1.1, 12 MBaud full speed, device mode
<b>UART</b>	16550-compatible, max. 3 MBaud, RTS / CTS support, Quantity 3
<b>I<sup>2</sup>C</b>	Master and Slave mode, 50 KHz up to 3.4 MHz, 16-bit FIFO, Quantity 2
<b>SPI / SQI with XiP</b>	Master and Slave mode, max. 10 MHz, 3 chip-select signal, Quantity 1 / 1
<b>General IOs</b>	As multiplex matrix of the internal periphery controller / 3.3 V / 6 mA, Quantity 40
<b>Status LEDs</b>	LEDs dual colored, 3.3 V / 9 mA, Quantity 2
<b>Memory bus</b>	32-bit data bus / 24-bit address bus
<b>Address range</b>	256 MByte SDRAM
<b>Memory components</b>	SDRAM or SRAM
<b>Dual-Port-Memory-Mode</b>	In part, the modes can be operated in parallel with an 8- or 16-bit data bus range. 8 / 16 / 32-bit data bus, 64 KByte configurable in 8 blocks, emulated via internal RAM
<b>Extension-Mode</b>	8 / 16 / 32-bit data bus, 24-bit address bus, adjustable bus timing
<b>SPI-Mode</b>	Slave with integrated Read/Write controller of the DPMs, 125 MHz
<b>MII-Mode</b>	Signals of the MII interface mapped in host interface
<b>SDRAM Mode</b>	16 / 32-bit SDRAM, max. 64 MByte
<b>PIO-Mode</b>	Freely programmable inputs and outputs, Quantity 53
<b>JTAG</b>	ARM processor and boundary scan
<b>ETM</b>	Embedded Trace Macrocell, ETM9 V2 medium size
<b>System cycle</b>	100 MHz
<b>Signal level</b>	+3.3 V
<b>Power supply</b>	for the core: +1.5 V   for inputs/outputs: +3.3V
<b>Operating temperature</b>	without heat sink: -40 ... +70 °C   with heat sink 10°/W: -40 ... +85 °C
<b>Storage temperature</b>	-65 ... +150 °C
<b>Power consumption</b>	PHYs switched off, typically: +0.8 W   PHYs switched on, typically: +1.5 W
<b>Housing</b>	PBGA, 1 mm raster: 324 Pins
<b>Dimensions (L x W)</b>	19 × 19 mm

Note: All technical data may be changed without further notice.

## Article Overview

### NETX 51

2231.001 | netX 51 Network Controller\*

\* When using a Hilscher Master Protocol, a Master license must be separately ordered. It will be delivered in the form of a Security EPROMs, and is foreseen for the design. For further information, please refer to [www.hilscher.com](http://www.hilscher.com)



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