Description

- 32Bit/100MHz ARM CPU and additional 32Bit/100 MHz RISC peripheral controller for parallel-signal processing, as PLC core, motion or IO-Link controller
- All field buses or Ethernet with integrated PHY and IEEE1588
- Single chip solution requires only one serial Flash EPROM
- DPM or SPI host interface
- Debug unit with USB connection
- Eclipse development environment
- Guaranteed delivery for 10 years

The netX 10 has a tri-core architecture with a central 32-Bit/100 MHz ARM CPU, a 32-Bit/100 MHz RISC controller as communication system for all field buses or as an Ethernet port and a further 32-Bit/100 MHz RISC controller for fast signal processing. It functions as a compact single chip solution in automated devices with network connection, such as O/Is, drives, sensors or ID systems. The Protocol Execution Controller xPEC is adapted by replacing the microcode on the determining processing of the status machine protocol and the communication functions of the respective network.

In contrast to this, the Peripheral Interface Controller xPIC can be freely programmed by the user and allows a fast signal processing parallel to the ARM-CPU, e.g. as motion or PLC core with CoDeSys or as intelligent IO-Link controller. The xPIC can access the entire address space of the netX 10 and with its second register base achieves an interrupt latency time of only 50 nanoseconds on external signals. The command set includes all standard RISC instructions, expanded by a 32x32 bit multiplication, fast loop logic and saturation support, which is all carried out in one cycle. All processor cores are connected via a central data switch with the internal RAM, the memory controller and the two peripheral buses. The general peripheral units, such as GPIO, timer, interrupt controller, UART, USB, SPI, I2C and the AD converter, encoder, PWMs for signals and outputs are distributed on these. The memory bus guided from this can be configured as a Dual Port Memory for connection to a Host CPU, as memory controller for SRAM and SDRAM or as simple PIOs. The SPI mode of the DPM’s enables a fast serial access to the internal memory.

The program code is loaded via the SPI interface in the internal SRAM and in SQI mode enables an ‘Execution in Place’ of the program code directly from the serial Flash EPROM. A Cordic unit is implemented for fast calculation of transcendent functions (some exponential functions, logarithms, sine and cosine).

With xPIC and the separate peripheral bus an independent IO or motion function block can be installed. All function units can be synchronized with each other.

24 signals can be selected from the periphery block via the internal multiplexer and reducing the BGA housing to 13x13 mm with 197 connections. The netX 10 is specified for the expanded temperature range and has guaranteed delivery for ten years. Using the standardized JTAG and ETM Interface (Embedded Trace Macrocell) all market available ARM development tools can be connected. Based on the Eclipse, there is a complete development environment with C compiler and comfortable operating of the internal debug unit with single step and break points via USB available.
Technical Specifications

Computer core
- Processor: ARM 966E-S, 100 MIPS, ARMv5TE command statement with DSP expansion
- Tightly coupled memory: 8 kbyte data, 8 kbyte commands

Internal memory
- RAM: 296 Kbyte divided into 4x64KB / 1x32KB /1x8KB memory blocks for parallel access to the processor core
- ROM: 64 Kbyte with Bootloader

Interrupt controller
- Processor: xPIC, 100MIPS, RISC, command statement with 32 x 32 bit multiplication, saturation support, fastloop logic
- Tightly coupled memory: 8 kbyte data, 8 kbyte commands
- Interrupt reaction time: 50 ns on external events by switching to second register bank

Ethernet-Interface
- Port: 1 x 10BASE-T / 100BASE-TX, Half-/ Full-Duplex, IEEE 1588 time stamp
- PHY: Integrated, auto negotiation, auto crossover
- Real-Time-Ethernet: EtherCAT, Modbus IDA

Fieldbus-Interface
- Instead of Ethernet each channel can be configured as a field bus controller.
- Fieldbus: CANopen, CC-Link, CompoNet, DeviceNet, PROFIBUS

Peripheral components
- Input link controller: 4 channels, controlled via xPIC
- IEEE 1588 system time: 32 bit second counter, 32 bit. nanosecond counter
- USB: Revision 1.1, 12 Mbaud Full-Speed, Device-Mode
- UART: 2x 16550 compatible max. 3 MBaud, RTS / CTS support
- SPI Master and Slave: 3.4 MHz
- ADC: 2x 8 channels/ Sample / Hold / PWM / programmable sequencer for interrupt and synchronization
- Encoder: 2 channels/ Filter / Capture / supports precise speed measurement / Interrupt / Synchronization
- CORDIC: Function accelerator for transcendental functions / polar acc. to Cartesian coordinate transformation
- General I/Os: 24x3.3V/6 mA
- Status LEDs: 2 LEDs two color, 3.3 V / 9 mA

Host-Interface
- Memory mode: 8/16-bit data bus / 24-bit address bus
- Address range: 64 MByte SDRAM and 16 MByte SRAM / Flash
- Dual-Port-Memory-Mode: 8 / 16-bit data bus, configurable from 2 to 128 KByte, emulated by internal RAM
- SPI Slave mode with up to 80 MHz transmission cycle
- Extension-Mode: 8/16-bit data bus, 24-bit address bus, bus timing adjustable
- PIO-Mode: 47x /freely programmable inputs and outputs

Debug-interface
- JTAG: ARM processor and boundary scan
- ETM: Embedded Trace Macrocell, ETM9 V2 Medium Size
- USB: Access to internal debug unit with single step and 2 hardware break points

Operating conditions/ Housing/ Miscellaneous data
- System cycle: 100 MHz ARM / 100 MHz peripheral
- Signal level: V
- Power supply: 1.5 V
- Operating temperature: °C
- Storage temperature: °C
- Power consumption: PHY switched off / Program code in internal SRAM
- Housing: FBGA, 0.6 mm raster

Product overview

<table>
<thead>
<tr>
<th>Article Description</th>
<th>Article Number</th>
<th>Article</th>
</tr>
</thead>
<tbody>
<tr>
<td>netX 10</td>
<td>2250.000</td>
<td>netX 10 network controller</td>
</tr>
<tr>
<td>NXHX 10-ETM</td>
<td>7753.200</td>
<td>netX 10 software development board</td>
</tr>
<tr>
<td>NXHX 10-IOL</td>
<td>7753.640</td>
<td>netX 10 I/O link evaluation board</td>
</tr>
</tbody>
</table>

Note: All technical data is provisional and can be changed without further notice.