



Device Description

**NDCM 100-NET**  
**netX DIMM Module**

Edition: 3

Language: English (EN)

**Hilscher Gesellschaft für Systemautomation mbH**

Web: [www.hilscher.com](http://www.hilscher.com)

# List of Revisions

Index	Date	Version	Chapter	Revisions
1	14.12.06	1	all	created
2	13.04.07	1	2.2	Added information about the system connector
3	25.05.07	1	5	Technical data fieldbus: CAN, DeviceNet, PROFIBUS

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We reserve the right to modify our products and their specifications at any time in as far as this contribute to technical progress. The version of the manual supplied with the device applies.

# Table of Contents

1	DESCRIPTION.....	4
1.1	Introduction .....	4
1.2	Overview NDCM100-NET.....	5
2	CONNECTORS.....	7
2.1	JTAG Board-to-Board-Connector .....	7
2.2	netDIMM Pinning NDCM 100-NET .....	8
3	SIGNAL DESCRIPTION NDCM 100-NET.....	12
3.1	Power.....	12
3.2	General Signals .....	13
3.3	Host interface signals .....	14
3.4	Standard interface signals .....	16
3.4.1	SPI Interface.....	16
3.4.2	USB Interface .....	17
3.4.3	UARTs / GPIOs .....	17
3.5	Ethernet Signals .....	19
3.6	XMAC Signals (Fieldbus).....	21
3.7	PWM Signals .....	23
3.8	AD Converter Signals .....	24
4	INDICATORS .....	25
5	TECHNICAL DATA NDCM 100-NET .....	26
6	MECHANICAL DIMENSIONS .....	27
7	LISTS .....	28
7.1	List of Figures .....	28
7.2	List of Tables .....	28

# 1 Description

## 1.1 Introduction

The netX DIMM Module is a CPU module in the well known DIMM form factor, featuring a netX communication controller, which allows quick and easy implementation of Real Time Ethernet communication and standard fieldbus interfaces.

Being a complete and already fully tested CPU system, integrating Flash- and RAM memory, crystal, reset generator and DC/DC converter, the NDCM100-NET frees the hardware designer from all the common obstacles that usually come with an own CPU hardware design, allowing the use of simple (down to 2 Layer PCBs, depending on application) custom application boards (baseboards) that usually only host the required connectors and physical interfaces for Ethernet and fieldbus interfaces, hence reducing design and product cost and time-to-market.

For evaluation purposes, a starter board is available, providing a connector to host the netDIMM Module. The netDIMM Starter Board comes with interfaces for Ethernet, PROFIBUS and DeviceNet and has RS232C, USB and JTAG connectors on-board. The extension bus of the DIMM Module is available through headers for ribbon cables.

The Starter Board comes with a power supply. All together, the Starter Board has everything needed to start developing and debugging own application software.



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### NOTICE

#### Device Destruction!

- Though the NDCM100-NET has the same form factor as a DIMM-PC™, it is **neither** pin compatible to the DIMM-PC™ standard, **nor** may it be powered by a 5V power supply! The NDCM100-NET may only be powered by a **3.3 V** power supply. Using the NDCM100-NET in any application board designed for DIMM-PC™s or the use of a higher supply voltage than 3.3V may result in severe damage to the module! Further, all signal pins require 3.3 V signaling voltage and are **not** 5V tolerant!

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*DIMM-PC™ is a registered trademark of Kontron AG*



The block diagram shows the netDIMM Module together with the starter board.

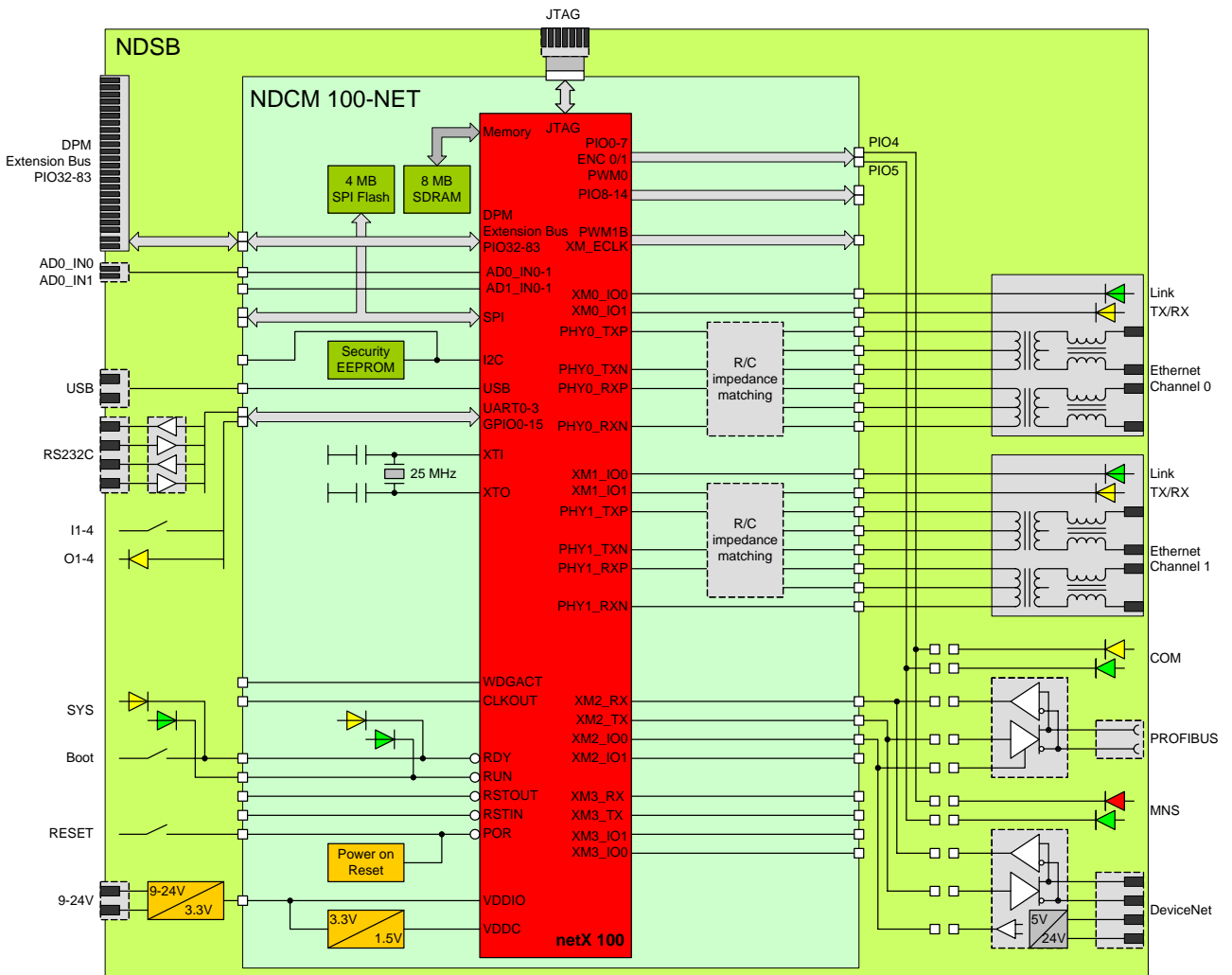


Figure 2: Block Diagram netDIMM NDCM 100-NET and netDIMM Starter Board NDSB-NET

## 2 Connectors

### 2.1 JTAG Board-to-Board-Connector

The NDCM modules provide their JTAG Interface through an 8 pin flex cable connector (X2), located near the upper left corner of the module.

**NOTE:** when inserting the flex cable, the contact sides of the cable must face the printed circuit board (connector has bottom contacts)!

Pin	JTAG Signals	netX Signals
1	+3.3V	+3.3V
2	GND	GND
3	TCLK	JT_TCLK
4	TDO	JT_TDO
5	TDI	JT_TDI
6	TMS	JT_TMS
7	TRSTN	JT_TRSTN
8	GND	GND

Table 1: JTAG connector, X2

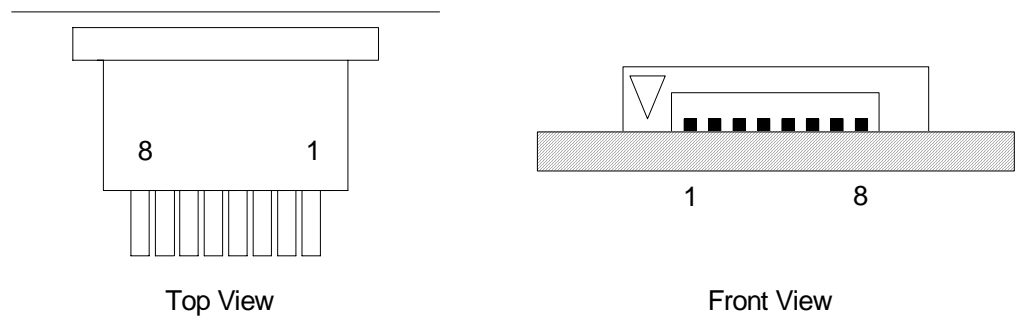


Figure 3: JTAG connector, X2

## 2.2 netDIMM Pinning NDCM 100-NET

Pin	General	Ext. Bus	Prog. I/O	DPM
1	+3V3			
2	GND			
3	PWM0E_U / ENC0_A		PIO0	
4	PWM0E_Un / ENC0_B		PIO1	
5	PWM0E_V / ENC0_N		PIO2	
6	PWM0E_Vn / ENC1_A		PIO3	
7	PWM0E_W / ENC1_B		PIO4	
8	PWM0E_Wn / ENC1_N		PIO5	
9	PWM0E_FAILn / ENC_MP0		PIO6	
10	PWM0E_RSV / ENC_MP1		PIO7	
11			PIO8	
12			PIO9	
13			PIO10	
14			PIO11	
15			PIO12	
16			PIO13	
17			PIO14	
18	XM0_ECLK / PWM1B_RSV			
19	XM1_ECLK / PWM1B_W			
20	XM2_ECLK / PWM1B_FAILn			
21	UART0_RXD		GPIO00	
22	UART0_TXD		GPIO01	
23	UART0_CTS		GPIO02	
24	UART0_RTS		GPIO03	
25	UART1_RXD		GPIO04	
26	UART1_TXD		GPIO05	
27	UART1_CTS		GPIO06	
28	UART1_RTS		GPIO07	
29	UART2_RXD		GPIO08	
30	UART2_TXD		GPIO09	
31	UART2_CTS		GPIO10	
32	UART2_RTS		GPIO11	
33			GPIO12	
34			GPIO13	
35			GPIO14	
36	IRQ		GPIO15	
37	XM2_IO1			
38	XM2_IO0			
39	XM2_RX			
40	XM2_TX			
41	XM1_IO1 // ETH1 Act LED			
42	PHY1_RXN			
43	XM1_IO0 // ETH1 Link LED			

*Continued on next page.*

Pin	General	Ext. Bus	Prog. I/O	DPM
44	PHY1_RXP			
45	XM0_IO1 / ETH0 Act LED			
46	PHY1_TXN			
47	XM0_IO0 / ETH0 Link LED			
48	PHY1_TXP			
49	PHY1_RXTAP			
50	PHY0_RXN			
51	PHY1_TXTAP			
52	PHY0_RXP			
53	PHY0_RXTAP			
54	PHY0_TXN			
55	PHY0_TXTAP			
56	PHY0_TXP			
57	USB_DPOS			
58	USB_DNEG			
59	+3V3			
60	GND			
61	+3V3			
62	GND			
63		CLKOUT / TCLK		
64	RDY			
65	RSTINn			
66	RUN			
67	RSTOUTn			
68	N.C.			
69	PORn			
70	WDGACT			
71		EXT_ALE	PIO35	
72			PIO36	
73		EXT_BHEn	PIO43	DPM_BHEn
74		EXT_WRHn	PIO44	DPM_WRHn
75		EXT_WRLn	PIO45	DPM_WRLn
76		EXT_RDn	PIO52	DPM_RDn
77		EXT_RDY	PIO46	DPM_RDY
78		EXT_IRQ	PIO47	DPM_INT
79		EXT_CS0n	PIO51	DPM_CSn
80		EXT_CS1n	PIO80	SEL_A17
81		EXT_CS2n	PIO79	SEL_A16
82		EXT_CS3n	PIO84	SEL_A18
83		EXT_A00	PIO73	DPM_A00
84		EXT_A01	PIO70	DPM_A01

*Continued on next page.*

Pin	General	Ext. Bus	Prog. I/O	DPM
85		EXT_A02	PIO69	DPM_A02
86		EXT_A03	PIO66	DPM_A03
87		EXT_A04	PIO65	DPM_A04
88		EXT_A05	PIO64	DPM_A05
89		EXT_A06	PIO61	DPM_A06
90		EXT_A07	PIO60	DPM_A07
91		EXT_A08	PIO57	DPM_A08
92		EXT_A09	PIO56	DPM_A09
93		EXT_A10	PIO53	DPM_A10
94		EXT_A11	PIO50	DPM_A11
95		EXT_A12	PIO49	DPM_A12
96		EXT_A13	PIO48	DPM_A13
97		EXT_A14	PIO54	DPM_A14
98		EXT_A15	PIO55	DPM_A15
99		EXT_A16	PIO58	(DPM_A16)
100		EXT_A17	PIO59	(DPM_A17)
101		EXT_A18	PIO62	(DPM_A18)
102		EXT_A19	PIO63	(DPM_A19)
103		EXT_A20	PIO67	SEL_A12
104		EXT_A21	PIO68	SEL_A13
105		EXT_A22	PIO71	SEL_A14
106		EXT_A23	PIO72	SEL_A15
107		EXT_A24	PIO40	SEL_A19
108		EXT_D00	PIO83	DPM_D00
109		EXT_D01	PIO82	DPM_D01
110		EXT_D02	PIO81	DPM_D02
111		EXT_D03	PIO78	DPM_D03
112		EXT_D04	PIO77	DPM_D04
113		EXT_D05	PIO76	DPM_D05
114		EXT_D06	PIO75	DPM_D06
115		EXT_D07	PIO74	DPM_D07
116		EXT_D08	PIO32	DPM_D08
117		EXT_D09	PIO34	DPM_D09
118		EXT_D10	PIO33	DPM_D10
119		EXT_D11	PIO39	DPM_D11
120		EXT_D12	PIO38	DPM_D12
121		EXT_D13	PIO37	DPM_D13
122		EXT_D14	PIO42	DPM_D14
123		EXT_D15	PIO41	DPM_D15
124	SPI_CLK			
125	SPI_MISO			
126	SPI_MOSI			

Continued on next page.

Pin	General	Ext. Bus	Prog. I/O	DPM
127	SPI_CS2n			
128	SPI_CS1n			
129	I2C_SCL			
130	I2C_SDA			
131	XM3_ECLK / PWM1B_Wn			
132	XM3_IO0 / PWM1B_V			
133	XM3_IO1 / PWM1B_Vn			
134	XM3_RX / PWM1B_U			
135	XM3_TX / PWM1B_Un			
136	ADC1_IN0			
137	ADC1_IN1			
138	ADC0_IN0			
139	ADC0_IN1			
140	ADC0_VDDIO			
141	ADC0_VREFP			
142	ADC0_VSS			
143	N.C.			
144	GND			

Table 2: netDIMM Pinning NDCM 100-NET

Information about the connector:

On the starter board NDSB-NET the connector Molex 54698-7001 is used to connect the NDCM 100-NET.

## 3 Signal Description NDCM 100-NET

Most signals of the NDCM 100-NET are directly connected to corresponding pins of the netX chip. For any signal details, not covered by this signal description, please consult the *netX Product Brief* and the *netDIMM Design Guide (not yet released)*.

### 3.1 Power

#### GND

All Ground Pins of the module shall be connected to the ground plane of the baseboard.

#### +3V3

All +3V3 Pins of the module shall be connected to the +3.3V power plane of the baseboard.

## 3.2 General Signals

### PORn

This is an active low bidirectional reset signal that can be used to automatically reset circuitry on the base/applicationboard during power up or brown-out situations. It can also be used to apply a power on reset to the NDCM 100-NET (for example reset button on baseboard). When using this signal as an input to the NDCM 100-NET, please note that the source for this signal must be an open collector or open drain output in order to avoid collision with the onboard reset generator of the module.

Further, as this signal is routed directly to the netX PORn input and does not trigger the onboard reset generator of the module, developers must take care, that the provided reset signal is “clean” (bounce free) and complies with the netX reset signal specifications (duration) as stated in the *netX Technical Reference Guide*.

### RDY

This bidirectional signal can either be used to output netX status information or to select certain netX boot modes (together with the RUN signal). It is connected to the netX RDY pin, parallel to the yellow LED of a dual LED located on the module.

### RUN

This bidirectional signal can either be used to output netX status information or to select certain netX boot modes (together with the RDY signal). It is connected to the netX RUN pin, parallel to the green LED of a dual LED located on the module.

### WDGACT

Active high output signal of the netX Watchdog unit.

### 3.3 Host interface signals

These signals can either be inputs, outputs, bidirectional signals or PIOs, depending on the module firmware. Although Hostinterface signals on the netX basically **can** be made 5V tolerant (by powering the appropriate power pin with 5V), they are **fixed** to **3.3V** signalling voltage on the NDCM 100-NET!

When operating in Hostinterface mode (DPM or Extension Bus) any unused signals (e.g. certain address lines) can individually be set to PIO mode and used as PIOs.

#### **DPM\_D[15:0] / EXT\_D[15:0] / PIOs**

Data inputs (external write) and outputs (external read) in DPM mode or data outputs (netX write) and inputs (netX read) in Extension Bus mode or PIOs.

#### **DPM\_A[19:0], SEL\_A[19:12] / EXT\_D[24:0] / PIOs**

Address signals (inputs in DPM mode and outputs in Extension Bus mode) or PIOs. As the netX virtual DPM size is 64k, only address lines DPM\_A15 to DPM\_A0 are used for addressing the DPM, however instead of using the DPM\_CS signal, address lines DPM\_A19 to DPM\_A16 (or to DPM\_A15,14,13 or 12 if less than 64k is used) can be used to generate an internal DPM chip select signal by comparing these address lines either to a programmable register value or to signals applied to the SEL\_A19 to SEL\_A12 lines (possible application is a DIP Switch connected to the SEL\_Ax lines for base address selection (-> ISA Bus))

#### **AEN / EXT\_ALE / PIO35**

AEN signal (-> ISA Bus) in DPM mode or Adress Latch Enable signal in Extension Bus mode or PIO.

#### **DPM\_BHE<sub>n</sub> / EXT\_BHE<sub>n</sub> / PIO43**

Byte High Enable, active low (indicates access to upper Byte). Input in DPM mode, output in Extension Bus mode or PIO.

#### **DPM\_WRL<sub>n</sub> / EXT\_WRL<sub>n</sub> / PIO45**

Write Low Byte, active low (indicates write access to low or both bytes, depending on Firmware). Input in DPM mode, output in Extension Bus mode or PIO.

#### **DPM\_WRH<sub>n</sub> / EXT\_WRH<sub>n</sub> / PIO44**

Write High Byte, active low (indicates write access to upper byte). Input in DPM mode, output in Extension Bus mode or PIO.

**DPM\_RDn / EXT\_RDn / PIO52**

Read signal, active low. Input in DPM mode, output in Extension Bus mode or PIO.

**DPM\_RDY / EXT\_RDY / PIO46**

Ready or Wait signal, function and polarity programmable. Output in DPM mode, input in Extension Bus mode or PIO.

**DPM\_CS<sub>n</sub> / EXT\_CS<sub>0n</sub> / PIO51**

Chip Select Signal, active low. Input in DPM mode, output in Extension Bus mode or PIO.

**EXT\_CS<sub>1n</sub> / PIO80**

Chip Select Signal, active low  
(active within Extension Bus memory window 1) or PIO.

**EXT\_CS<sub>2n</sub> / PIO79**

Chip Select Signal, active low  
(active within Extension Bus memory window 2) or PIO.

**EXT\_CS<sub>3n</sub> / PIO84**

Chip Select Signal, active low  
(active within Extension Bus memory window 3) or PIO.

**DPM\_INT / EXT\_IRQ / PIO47**

Interrupt signal, polarity programmable. Output in DPM mode, input in Extension Bus mode or PIO.

**CLOCKOUT**

Clock signal output, frequency programmable.

**RSTOUT<sub>n</sub>**

Reset signal output, programmable.

**PIO36**

PIO.

## 3.4 Standard interface signals

### 3.4.1 SPI Interface

**SPI\_CLK**

Clock signal of the SPI Interface.

**SPI\_MISO**

Master In Slave Out. SPI Data input signal from external SPI Devices.

**SPI\_MOSI**

Master Out Slave In. SPI Data output signal to external SPI Devices.

**SPI\_CS2n**

SPI chip select signal 2. Output, active low.

**SPI\_CS1n**

SPI chip select signal 1. Output, active low.

## 3.4.2 USB Interface

### USB\_DPOS

USB+ differential signal of the netX USB Interface.

### USB\_DNEG

USB- differential signal of the netX USB Interface. The USB signals are directly connected to appropriate netX interface pins without any further circuitry. All pullups / pulldowns and ESD protection are to be provided by the baseboard.

## 3.4.3 UARTs / GPIOs

UARTs and GPIOs share the same pins, while the functionality of each pin (UART or GPIO) is programmable individually. GPIO functions include PWM and interrupt functions. All UART signals are logic level signals (3.3V) and require RS-232 transceivers on the baseboard if standard serial ports are to be realized.

### UART0\_RXD / GPIO 0

Receive Data signal of UART0 (input) or GPIO.

### UART0\_TXD / GPIO 1

Transmit Data signal of UART0 (output) or GPIO.

### UART0\_CTS / GPIO 2

Clear To Send signal of UART0 (input) or GPIO.

### UART0\_RTS / GPIO 3

Request To Send signal of UART0 (output) or GPIO.

### UART1\_RXD / GPIO 4

Receive Data signal of UART1 (input) or GPIO.

### UART1\_TXD / GPIO 5

Transmit Data signal of UART1 (output) or GPIO.

**UART1\_CTS / GPIO 6**

Clear To Send signal of UART1 (input) or GPIO.

**UART1\_RTS / GPIO 7**

Request To Send signal of UART1 (output) or GPIO.

**UART2\_RXD / GPIO 8**

Receive Data signal of UART2 (input) or GPIO.

**UART2\_TXD / GPIO 9**

Transmit Data signal of UART2 (output) or GPIO.

**UART2\_CTS / GPIO 10**

Clear To Send signal of UART2 (input) or GPIO.

**UART2\_RTS / GPIO 11**

Request To Send signal of UART2 (output) or GPIO.

**GPIO [15:12]**

GPIOs.

## 3.5 Ethernet Signals

The module already contains all necessary pullup / pulldown resistors and capacitors for the chip side of the Ethernet Interface. The baseboard only has to provide appropriate Transformers (see netDIMM Design Guide for details).

### **PHY0\_RXN**

Neg. differential Receive signal of Ethernet Channel 0.

### **PHY0\_RXP**

Pos. differential Receive signal of Ethernet Channel 0.

### **PHY0\_RXTAP**

Connects to the center tap of the Ethernet Transformers Receive winding for Channel 0 (Transformer is located on the baseboard).

### **PHY0\_TXN**

Neg. differential Transmit signal of Ethernet Channel 0.

### **PHY0\_TXP**

Pos. differential Transmit signal of Ethernet Channel 0.

### **PHY0\_TXTAP**

Connects to the center tap of the Ethernet Transformers Transmit winding for Channel 0 (Transformer is located on the baseboard).

### **PHY1\_RXN**

Neg. differential Receive signal of Ethernet Channel 1.

### **PHY1\_RXP**

Pos. differential Receive signal of Ethernet Channel 1.

### **PHY1\_RXTAP**

Connects to the center tap of the Ethernet Transformers Receive winding for Channel 1 (Transformer is located on the baseboard).

**PHY1\_TXN**

Neg. differential Transmit signal of Ethernet Channel 1.

**PHY1\_TXP**

Pos. differential Transmit signal of Ethernet Channel 1.

**PHY0\_TXTAP**

Connects to the center tap of the Ethernet Transformers Transmit winding for Channel 0 (Transformer is located on the baseboard).

## 3.6 XMAC Signals (Fieldbus)

### **XM2\_RX**

Receive Data signal of XMAC2 Channel.

### **XM2\_TX**

Transmit Data signal of XMAC2 Channel.

### **XM2\_IO0**

I/O signal 0 of XMAC2 Channel.

### **XM2\_IO1**

I/O signal 1 of XMAC2 Channel.

### **XM2\_ECLK**

External XMAC clock signal (I/O) of XMAC2 Channel.  
(currently unused, reserved for future use)

### **XM3\_RX**

Receive Data signal of XMAC3 Channel.

### **XM3\_TX**

Transmit Data signal of XMAC3 Channel.

### **XM3\_IO0**

I/O signal 0 of XMAC3 Channel.

### **XM3\_IO1**

I/O signal 1 of XMAC3 Channel.

### **XM3\_ECLK**

External XMAC clock signal (I/O) of XMAC3 Channel.  
(currently unused, reserved for future use)

**XM0\_IO0**

I/O signal 0 of XMAC0 Channel.

**XM0\_IO1**

I/O signal 1 of XMAC0 Channel.

**XM0\_ECLK**

External XMAC clock signal (I/O) of XMAC0 Channel.  
(currently unused, reserved for future use)

**XM1\_IO0**

I/O signal 0 of XMAC0 Channel.

**XM1\_IO1**

I/O signal 1 of XMAC0 Channel.

**XM1\_ECLK**

External XMAC clock signal (I/O) of XMAC1 Channel.  
(currently unused, reserved for future use)

**Note:**

The XMAC I/O signals of XMAC0 and XMAC1 are destined to be used to drive the Activity and Link Status LEDs of Ethernet channels 0 and 1 (signals are active low).

## 3.7 PWM Signals

These signals can either be XMAC signals or PWM (PWM module 1B) signals, depending on the module firmware.

### **PWM1B\_U**

PWM signal U (phase 1 of 3-phase PWM).

### **PWM1B\_Un**

PWM signal U, inverted.

### **PWM1B\_V**

PWM signal V (phase 2 of 3-phase PWM).

### **PWM1B\_Vn**

PWM signal V, inverted.

### **PWM1B\_W**

PWM signal W (phase 3 of 3-phase PWM).

### **PWM1B\_Wn**

PWM signal W, inverted.

### **PWM1B\_FAILn**

Failure Input for PWM. When this signal is active (low), all PWM Outputs will automatically be disabled!

### **PWM1B\_RSV**

PWM signal for Resolver.

## 3.8 AD Converter Signals

### ADC0\_IN0

Analog input for ADC 0, Channel 0

### ADC0\_IN1

Analog input for ADC 0, Channel 1

### ADC1\_IN0

Analog input for ADC 1, Channel 0

### ADC1\_IN1

Analog input for ADC 1, Channel 1

### ADC0\_VDDIO

+3.3V ADC supply voltage (filtered). Can be used to power additional analog circuits (max. 150mA) on the baseboard. **Do not connect a power source to this signal!**

### ADC0\_VREFP

ADC reference voltage (connected to ADC0\_VDDIO through 10k serial resistor). Can be used as reference for additional analog circuits on the baseboard or to apply a different reference voltage supplied by an external source.

### ADC0\_VSS

Analog Ground.

## 4 Indicators

The NDCM 100-NET provides an onboard Dual LED (yellow / green) for status display purposes. This LED can be driven by the RDY and RUN signals which are also routed to the modules edge connector (see also 2.3.2. General Signals).

LED	Color	State	Indicates
SYS	yellow	Flashing cyclic with 1Hz	Device is in bootstraploader mode and waiting for firmware download
	yellow	On / Off	Device may have detected monitor connection through serial or USB
	yellow		Once a firmware is loaded, it has complete control over the SYS LED states. Hence, the functionality of the SYS LEDs is application/firmware specific.
	green		

*Tabelle 1: Module States LED V1*

## 5 Technical Data NDCM 100-NET

### Technical data hardware

Parameter	Value / Range
Processor	netX 500 with 200 MHz ARM926EJ-S
Memory	4 MByte SPI Flash, 8 MByte SDRAM,
Standard Interfaces	USB 1.1, SPI, 3x UART or 16x GPIO, JTAG
AD-Converter	2 * 2 Channels (multiplexed), 10-Bit, 1 MS/s, S&H
2 Ethernet-Ports	10BASE-T/100BASE-TX, integrated PHYs
Hostinterface	Dual-Port Memory up to 64 KByte or Extension Bus or 52 x IO
Power Supply	+3,3 V $\pm$ 5 % / 750 mA
Dimensions (L x W x T)	67.6 x 40 x 2.8 mm (mechanically complies with DIMM Standard)
Operating Temperature	-25 °C ... 55 °C (can be extended to + 70°C by using an optional heat sink)

Table 3: Technical Data Hardware NDCM 100-NET

### Special features for communication protocols

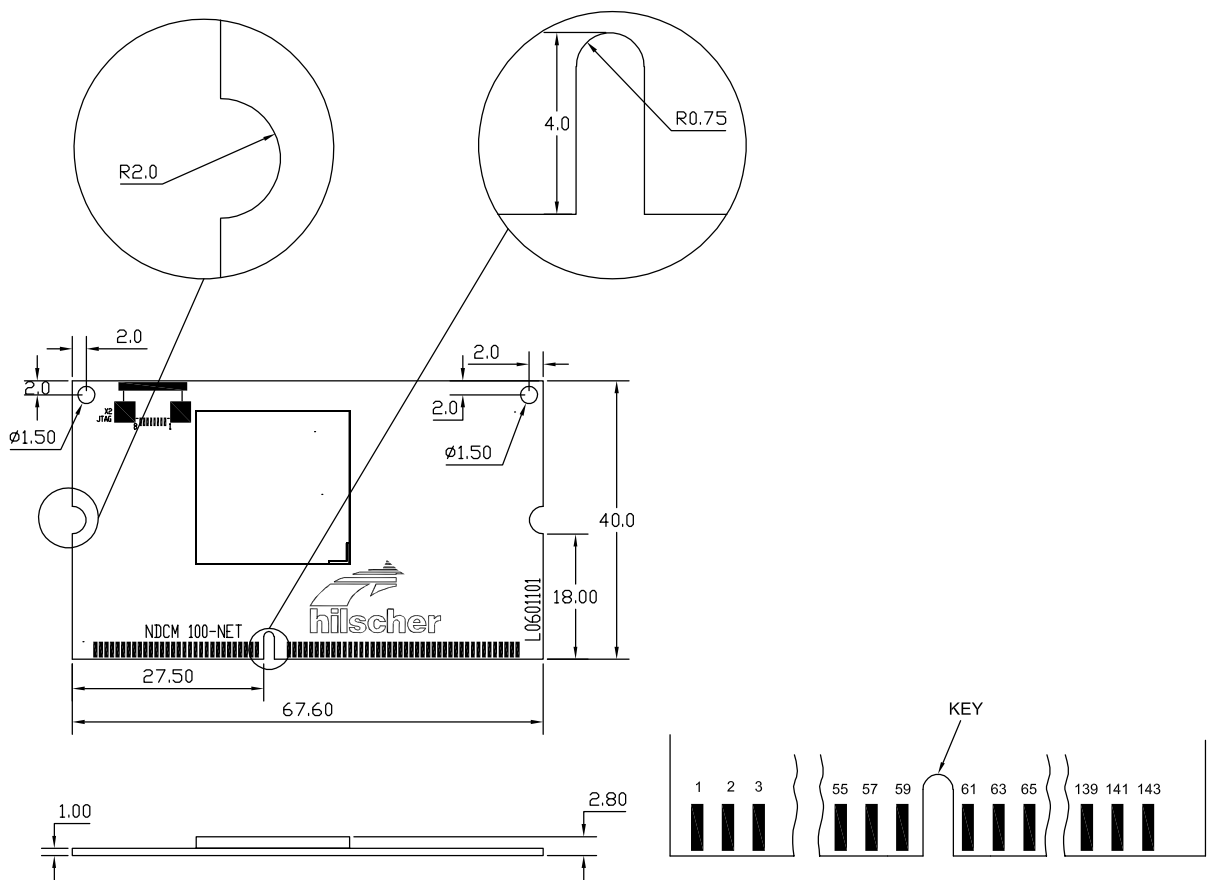
Parameter	Value / Range
2 Ethernet-Ports	IEEE 1588 EtherCAT with 3 FMMUs and 4 SyncManager EtherNet/IP Powerlink, integrated Hub, Response Delay max.1 $\mu$ s PROFINET, integrated Switch SERCOS III
Fieldbus Controller	CAN, DeviceNet, PROFIBUS

Table 4: Basic Technical Data for communication protocols NDCM 100-NET

The special features are only usable with the corresponding protocol stack.

# 6 Mechanical Dimensions

- all dimensions in mm -



## 7 Lists

### 7.1 List of Figures

<i>Figure 1: Overview NDCM 100-NET</i>	5
<i>Figure 2: Block Diagram netDIMM NDCM 100-NET and netDIMM Starter Board NDSB-NET</i>	6
<i>Figure 3: JTAG connector, X2</i>	7

### 7.2 List of Tables

Table 1: JTAG connector, X2	7
Table 2: netDIMM Pinning NDCM 100-NET	11
Table 3: Technical Data Hardware NDCM 100-NET	26
Table 4: Basic Technical Data for communication protocols NDCM 100-NET	26