Device Description

NXDB 500-SYS

netX Development Board

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Hilscher Gesellschaft für Systemautomation mbH

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List of Revisions

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We reserve the right to modify our products and their specifications at any time in as far as this contribute to technical progress. The version of the manual supplied with the device applies.

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1 Description

1.1 Introduction

The NXDB500-SYS is a fully featured Developmentboard allowing the user to evaluate virtually any functionality provided by the netX 500 chip.

The board is equipped with all common Fieldbus Interfaces (CAN, Profibus, AS-i, Devicenet, InterBus and CC-Link) whereas one of these Interfaces can be used at a time.

Further, the board provides two 100Mbit Ethernet Ports for Realtime Ethernet communication.

As standard communication ports the user will find three RS-232 serial ports, whereas one of them can also be configured as an InfraRed (IrDA) Interface, as well as a USB (1.1. fullspeed) port which can either operate as Host or Device.

The memory setup of the board comes with external SDRAM, external parallel flash, external SRAM and NVRAM, SPI Flash, I2C EEPROM and a SD-Card (MMC) interface supporting standard SD memory cards.

All elements of the board are powered by an onboard switching power supply, which can be operated by a wide range of simple (unregulated) standard power supplies from 9V to 24V output voltage.

Equipped with an optional QVGA TFT display with Touchscreen, the graphics capabilities of the netX 500 can easily be evaluated. A standard 0.1” ribbon cable can be used to connect almost any external display (DSTN or TFT) instead of the onboard display.

The NXDB500-SYS also allows the user to install various extensions, yet increasing the wide range of functions already provided by the standard board. The extension capabilities include a DIMM socket, which can either host a standardized third party DIMM-PC or special Hilscher memory modules as they come available in the future.

For future fieldbus interfaces a reserved area on the board along with an appropriate connector is provided to connect either a user designed addon board or future extension modules from Hilscher.

A special prototyping area on the board allows the user to add custom circuits to the board, while standard 0.1” headers provide access to almost any relevant netX500 signal, either for measurement purposes or to connect custom hardware to the board.

For software development, all NXDB500-SYS come with a JTAG connector, allowing to connect an appropriate debugger device. If required, the board can also be equipped with an ETM connector to connect high end debugging units to the netX making use of the Embedded Trace Macrocell of the netX ARM CPU.

Windows CE and Linux board support packages are available from Hilscher, allowing to run any of these operating systems on the NXDB500-SYS.

1.2 Location of Connectors, Indicators and Control Elements

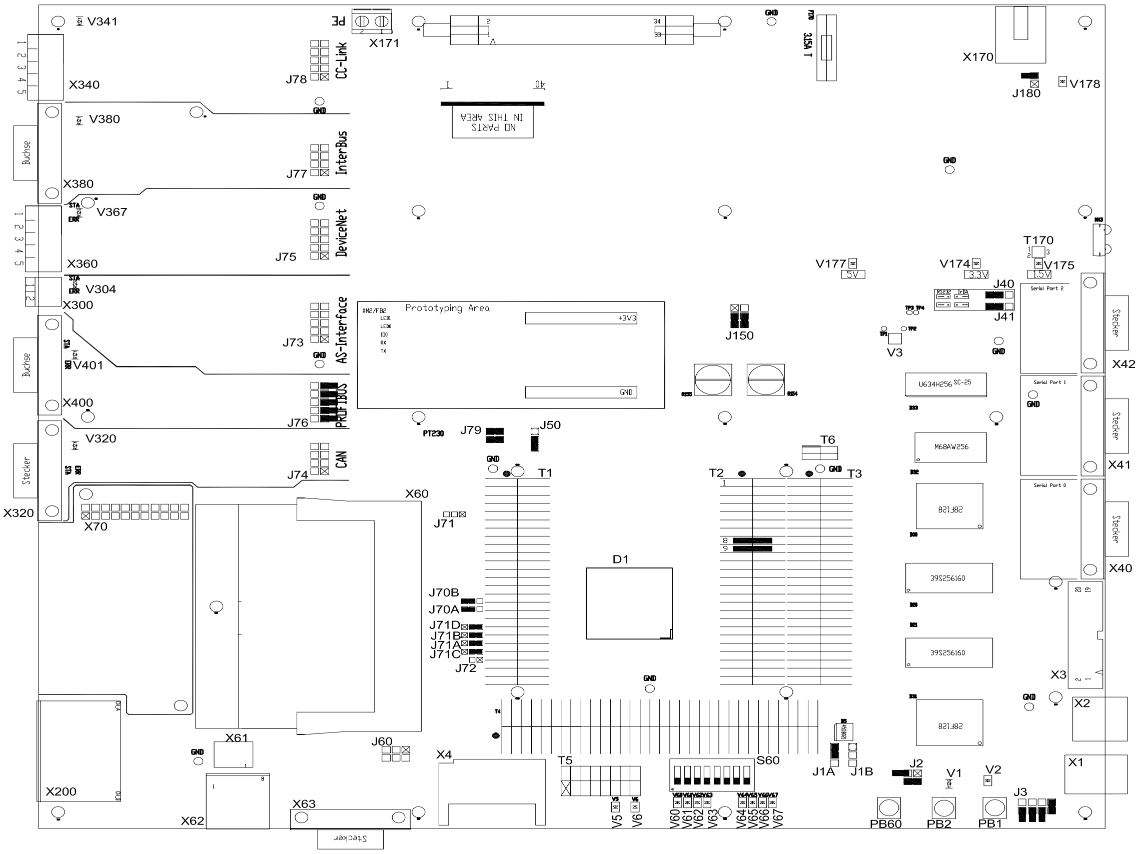

Figure 1: NXDB 500-SYS

2 Board Configuration and Operation

2.1 Boot Mode

The versatile boot options of the netX500 require proper setting of the desired boot mode of the board. In order to correctly set the desired boot mode, it is neccessary to understand the netx500 boot sequence:

Except when configured for Bootstart mode, the netx500 will allways search for executable boot code at the parallel flash, at memory connected to the SPI bus (CS0), the I2C Bus and the SD card interface. Once appropriate boot code is found in any of these devices, it will be executed. If no boot code is found, the configured boot mode comes in.

The following boot modes are available:

- Bootastart Boot Mode
- DPM Boot Mode
- Extension Bus Boot Mode

In Bootstart Boot Mode, the netX500 activates the serial port on UART0 and the USB port (requires configuring the USB port to “device mode”, see chapter 2.11) and waits for being contacted by an application running on an external host computer. An appropriate Windows Application, providing access to netX registers and memory for downloading program code, etc. is available from Hilscher. In bootstart mode, any connected bootable memory will be ignored.

In DPM Boot mMode, the Hostinterface of the netX500 will automatically be configured as a standard DPM. The netX500 then waits for an external host system to write appropriate boot code to the DPM which will then be executed.

In Extension Bus Boot Mode, the Hostinterface the netX500 will automatically be set to extension bus mode. The netX500 will then scan the extension bus for a connected parallel memory device (Flash, NVRAM, etc.) using the CS0n Extension bus chip select signal that contains appropriate boot code.

The boot mode is configured by Jumper J2, which is located near the lower right corner of the board. See Table 2.xx below for the different settings:

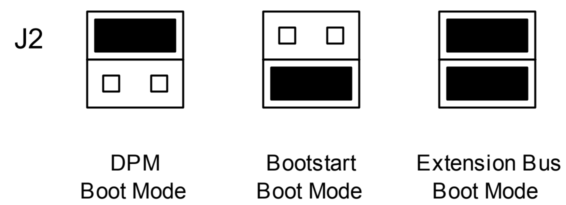

Figure 2: J2

If no jumper is set, the Bootstart button PB2 (the button in the middle of the pushbutton row at the lower edge of the board on the right side) can be used to enter the Bootstart mode.

If this button is held active (pressed) while a reset is applied to the board, the board will come up in Bootstart mode.

For further information on operating the NXDB500 in Bootstart mode, see also Chapter xx (First Steps). For additional information on the DPM and Extension bus boot mode, see appropriate netX documentation.

2.2 Reset

The NXDB500-SYS is equipped with an onboard reset generator, providing a proper Power On Reset signal to the netX500. This circuit will also issue a reset, in case the voltage from the onboard 3,3V power supply should drop below appr. 2,9V -3V.

Additionally, the netX can be manually reset by two different pushbuttons:

Button PB1 (the outer right button of the pushbutton row at the lower edge of the board on the right side, labelled “RESET”) will also activate the Power On Reset signal (signal remains active until button is released). While a “true “Power On Reset also activates the JTAG-Reset signal applied to the netX500 (Pin U17), the reset controlled by PB1, only activates the PORn signal which also resets the onboard Flash memories.

Button PB60 (the outer right button of the pushbutton row at the lower edge of the board on the right side, labelled “HIF-RESET”) activates another interrupt signal applied to the secondary interrupt input of the netX500 (Pin W19).

Basically, the netX500 can be manually reset by any of the two signals mentioned before, however the appropriate netX register which reflects the type of reset that occurred last, will be different (see appropriate netX documentation for details).

2.3 Power Supply / Power Fail

The NXDB500-SYS can be operated by a DC power supply from 9V – 24V which is to be plugged into the power jack X170 located in the upper right corner of the board.

As the input circuit provides a bridge rectifier, the polarity of the power plug does not matter, however an AC supply shall not be used, as the input capacitors are not sufficient for that mode of operation. The current drawn by the NXDB500-SYS depends on several factors such as operating mode of the netX500, CPU load, use of additional hardware and mainly on the level of the input voltage (the higher the voltage, the lower the current). For standard operation of the board, the power supply that comes with your NXDB500-SYS is sufficient. If additional hardware is used on the NXD500-SYS, the use of a stronger supply is recommended. To protect the input rectifier diodes, the board is equipped with a standard fuse (3.15 Amps., Time Lag).

The board provides a secondary voltage control circuit, which is connected to the input voltage of the board. This circuit will generate a Power Fail signal when the input voltage drops below 8.5 V. The Power Fail signal can be routed to the RTC_POK signal of the netX500, allowing evaluation of the isolated memory feature of the netx500.

An active Power Fail signal is indicated by LED V178 in the upper right corner of the board (next to the power in connector). Through jumper J100, located at the left side from V178, the signal can be connected to the RTC_POK input (pin W7) of the netx500. By default, the jumper is not set, leaving the RTC_POK in high level (RTC power is good).

2.4 JTAG

Through connector X3, located near the lower right corner of the board, the user has access to the JTAG interface of the integrated ARM CPU inside the netX500.

The connector pinout follows the common standard for ARM JTAG interfaces and can be found in chapter 5 of this manual.

The JTAG port allows the connection of appropriate debugging devices, such as the “Tantino” from Hitex or the “RealView Multi-ICE” available from ARM.

2.5 ETM

The NXDB500-SYS can be equipped with an optional ETM connector (X50), located almost in the center of the board, above the netx500 chip and provides access to the “Embedded Trace Macrocell” inside the ARM CPU. This interface allows low level debugging by the use of appropriate debugging units (for example “Tanto” available from Hitex).

If you need to upgrade your NXDB500-SYS with an ETM connector or wish to purchase a board already equipped with such a connector, please contact the Hilscher sales department.

2.6 Fieldbus Interfaces

The NXDB500-SYS provides a total of 6 different fieldbus interfaces (CAN, ProfiBus, AS-Interface, DeviceNet, InterBus and CC-Link) which can be connected to the netX500 and will then be operated by XMAX/XPEC**2**.

Every interface has a dual led, providing fieldbus status information.

Only one of these interfaces can be used at a time and the board must be configured appropriately in order to use a certain interface!

The interfaces are located on left side of the board from the upper corner down to approximately the middle of the board. There is one jumper group for each of the interface which are all vertically alligned.

Note ***In order to use a certain interface, ALL of the jumpers in the appropriate jumper group must be set (plugged), while ALL jumpers of the other groups must be removed! Setting jumpers in more than one group, will cause malfunction and may even damage the board, so configuration should be done very carefully and should be checked before powering up the board!***

The NXDB500-SYS also serves as a reference design for the netX500. Hence the idea of selecting the fieldbus interfaces through multiplexers, making the configuration more convenient and eliminating the possibility of misconfigurations, was dropped, in order to make the connection between netX and the “physical” part of the fieldbus interface as transparent as possible.

2.6.1 CANopen

The CANopen interface is the first interface starting from the middle of the left side of the board.

In order to use this interface, all 4 jumpers of jumper group J74 must be set as shown in the following picture.

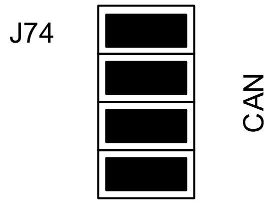

Figure 3: J74 - CAN

CAN devices are connected to the NXDB500-SYS through connector X320, a standard 9 pin SUB-D male connector.

2.6.2 PROFIBUS

The Profibus interface is the second interface starting from the middle of the left side of the board. In order to use this interface, all 5 jumpers of jumper group J76 must be set as shown in the following picture.

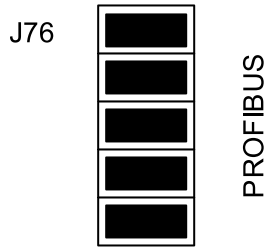

Figure 4: J76 - PROFIBUS

PROFIBUS devices are connected to the NXDB500-SYS through connector X400, a standard 9 pin SUB-D female connector.

2.6.3 AS-Interface

The AS-Interface is the third interface starting from the middle of the left side of the board. In order to use this interface, all 5 jumpers of jumper group J73 must be set as shown in the following picture.

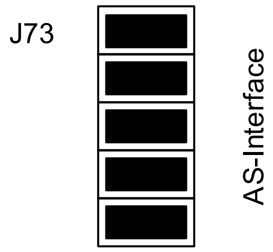

Figure 5: J73 - AS-Interface

AS-i devices are connected to the NXDB500-SYS through connector X300, a 2 pin Combicon connector.

2.6.4 DeviceNet

The DeviceNet -Interface is the fourth interface starting from the middle of the left side of the board. In order to use this interface, all 5 jumpers of jumper group J75 must be set as shown in the following picture.

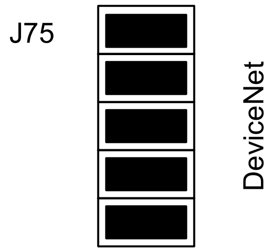

Figure 6: J75 - DeviceNet

DeviceNet units are connected to the NXDB500-SYS through connector X360, a 5 pin Combicon connector.

2.6.5 InterBus

The InterBus Interface is the fifth interface starting from the middle of the left side of the board. In order to use this interface, all 4 jumpers of jumper group J77 must be set as shown in the following picture.

Figure 7: J77 - AS-InterBus

DeviceNet units are connected to the NXDB500-SYS through connector X380, a a standard 9 pin SUB-D female connector.

2.6.6 CC-Link

The CC-Link -Interface is the first interface in the upper left corner of the board. In order to use this interface, all 4 jumpers of jumper group J77 must be set as shown in the following picture.

Figure 8: J78 - CC-Link

CC-Link units are connected to the NXDB500-SYS through connector X340, a 5 pin Combicon connector.

2.7 Ethernet Ports

The NXDB500-SYS provides two standard 100Mbit Ethernet ports combined in a double RJ-45 jack which are driven directly by the two internal PHYs of the netX500.

The jack is located in the lower left corner of the board and also contains Link- and Activity LEDs for both channels. The ethernet ports itself are hardwired on the board, however the status LEDs require proper setting of two jumpers, J70A and J70B.

These jumpers have already been set to their default position (1-2) by factory.

The deafult position is indicated on the silk screen of the board and is also shown in the following figure.

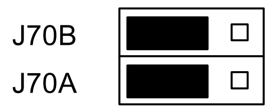

Figure 9: J70B / J70A

2.8 Xmax Clocks

The XMACs of the netX500 are usually clocked by a programmable internal clock source, however if required, all 4 XMACs can be clocked individually by external clock signals.

In normal mode (internal clocking), the four clock jumpers (J71A, J71B, J71C, J71D) are set to their default position (2-3), routing the clock inputs to to connector T1.

When one or more XMACs are to be clocked externally, the appropiate jumper can be set to position 2-3 (J71A : XMAC0, J71B : XMAC1, J71C : XMAC2, J71D : XMAC3).

The clock input(s) are then routed to J71 which again can connect this line to two different clock generators (G70 and G71). As external clocking is usually not necessary, the two landing patterns for the clock generators on the NXDB500-SYS are not populated, allowing the user to mount the required clock generators himself.

The XMAC Clock jumpers have already been set to their default position (2-3) by factory.

The default position is indicated on the silk screen of the board and is also shown in the following figure.

Figure 10: J71D / J71B / J 71A / J71C

2.9 UARTs

The three UARTs of the netX500 are connected through common RS-232 level shifters to three standard serial ports (RX,TX,RTS,CTS) located on the right side of the board.

One of these ports (UART2) can alternatively be used as an Infrared port (IrDA), by setting jumpers J40 and J41 from their default position (1-2) to position 2-3. (of course the IrDA port will not work unless UART2 has also been correctly configured for IrDA mode by software. The jumpers only provide the physical conection to the IrDA transceivers!)

Jumpers J40 and J41 are shown in the following picture.

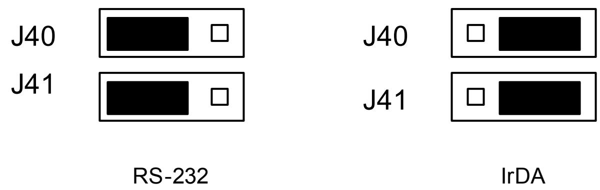

Figure 11: J40 / J41 - RS-232, J40 / J41 - IrDA

2.10 SPI Flash

The NXDB500-SYS is equipped with a serial (SPI) Flash memory (D5), that can either be connected to the SPI chip select 0 (SPI_CS0n) or the SPI chip select 2 signal (SPI_CS2n) of the netX500. The chip select signal is selected by Jumper **J1A** (see the figure below).

Further, the board provides an unpopulated landing pattern for an additional SPI Flash memory (D6) with a different package (standard SO-8) and pinout, which can be used to add another memory to the board, if required. Suitable components are for example SST25VF010, or SST25VF020 (please consult the board schematics, page 1 for details on the pinout).

If D6 is populated and both SPI memories are to be used, Jumper **J1B** must be used to also set the chip select signal for D6. The settings for J1A and J1B must be different!

If the NXDB500-SYS is to boot from SPI memory, the desired memory must be configured to use chip select 0 (SPI_CS0n).

If the SPI chip select signals are to be used for external SPI hardware, added to the board via the signal headers (chapter 4.1.4), then jumpers J1A and J1B should be removed to disable any onboard SPI memory.

Figure 12: J1A - SPI_CSO, J1A - SPI_CS2

2.11 USB

On the lower right corner of the NXDB500-SYS, there are two USB connectors (Type A and B) that are connected to the USB port of the netX500. The USB port can be configured to either operate as USB Host port or as USB device port by setting the jumpers of jumper group J3 accordingly (see figure below).

Although two connectors are available, only one of them (along with the proper jumper setting) may be used at a time! Also make sure, that no externally powered USB device (e.g. Host-PC) is connected to the board, while the NXDB500-SYS has no power supply connected, as this may cause damage to the USP port of the netX500!

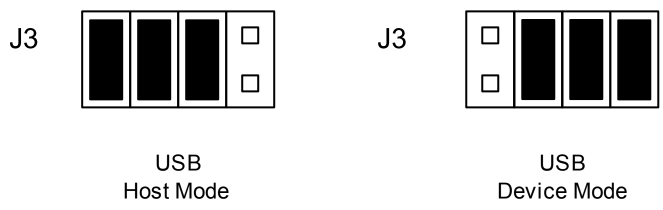

Figure 13: J3 - USB Host Mode, J3 - USB Device Mode

2.12 ADCs

The netX500 provides a total of 8 analog channels (2 * 4 multiplexed) which are all accessible via signal header T3. For quick evaluation of the ADCs, the NXDB500-SYS provides two potentiometers (R154 and R155) to generate two different voltages from 0V to 3.3V (U_ANA0 and U_ANA1). These voltages can be routed to one or more ADC channels by using jumpers on signal header T3.

By default, two of the ADC channels (ADC1, channel 2 and 3) are reserved for the touch panel of the integrated TFT Display on the NXDB500-SYS (see also chapter 2.13).

Please consult the board schematics (page 15) and the Interface Connector Pinout of T3 (chapter 5) for details.

2.13 LCD and Touchpanel

The NXDB500-SYS comes with an onboard QVGA (320*200) TFT Display with a 4-wire resistive touch panel which is supported by the available Windows CE and Linux board support packages.

By default, all jumpers have been set to enable display operation. For the display itself, only jumper **J50** is relevant, which must be set to position 2-3 (see figure below).

The NXDB500-SYS also allows the connection of other displays through a standard 34-pin ribbon cable, using connector **X52** which is located directly above the onboard display.

This connector provides access to all signals of the netX500 LCD Interface (see Interface Connector Pinout of X52 (chapter 5) for details).

When using an external display, the onboard display should be disconnected, by carefully removing the flat cable from connector X51, located under the display.

For touch panel operation, all relevant jumpers have already been set correctly by factory.

These jumpers and their required positions are listed as follows: J79 (positions 1-2 and 3-4), J150 (positions 3-5 and 4-6) and header T3 (positions 15-16 and 17-18) (see also figure below).

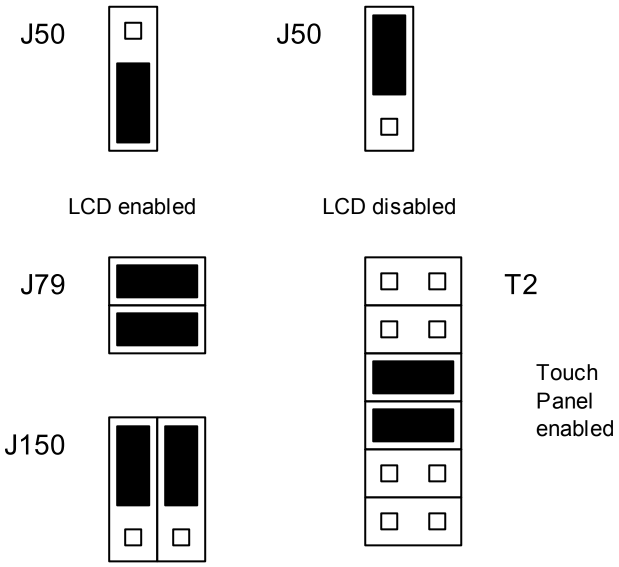

Figure 14: J50 - LCD enabled, J50 LCD disabled, J79 / J150, T2 - Touch Panel enabled

2.14 Host Interface-PIO LEDs / Switch

The NXDB500-SYS provides 8 LEDs (V60 – V67) and an 8 Bit DIP-Switch (S60) which are connected to I/O lines of the netx500 Hostinterface and serve several purposes.

For diagnostic purposes, some or all of the LEDs can be controlled by the netX500, if the corresponding I/O pins are configured as GPIO pins (see Program Reference Guide for details). In that case, the corresponding DIP Switch must also be set to the “ON” position, in order to connect the LED to the I/O pin.

The assignment between the LEDs / Switches and the HIF-GPIO pins are as follows:

LED	HIF-GPIO	netX500 pin
V60	67	D9
V61	68	E9
V62	71	D8
V63	72	E8
V64	79	D6
V65	80	E6
V66	84	D5
V67	40	E16

Table 1: Assignment LEDs / Switches - HIF-GPIO pins

As long as the Hostinterface has not been configured, all Host-Interface pins are floating (and are either pulled up or pulled down by week (22k) pullup / pulldown resistors (see schematics, page 6 for details)). Hence all LEDs that have been connected by the DIP Switch will be dim.

Whenever a pin is configured as GPIO, the LED will either be on (pin driven low) or completely turned off (pin driven high).

The second function of the DIP Switches comes in, when the corresponding pins are to be used as inputs. Setting a switch to the “ON” position will cause a high input level on the corresponding pin, while setting it to the “OFF” position, causes a low level.

As the levels caused by the switches are achieved by “week” pullups/pulldowns, they will allways be overridden by the level driven from pins configured as outputs.

The third function of the DIP Switch is related to the DPM mode of the netX500 Hostinterface. When the Hostinterface is configured as DPM, the DIP Switches can be used to externally configure the Base Adress of the virtual netX500 DPM.

3 LED Status Indicators

3.1 Power LEDs

The NXDB500-SYS has three green LEDs, located at the lower end of the power supply section of the board, which are labelled with “5V”, “3.3” and “1.5V”.

These LEDs provide a simple status information on the power supply, as they are lit, whenever the corresponding voltage is present. Please note, that these LEDs are simply driven by the corresponding power net and do not provide any information on the exact level or quality of the voltage.

3.2 RDY/RUN LEDs

Located near the lower right corner of the NXDD500-SYS, directly above the “BOOT” Pushbutton, there is a dual LED (yellow/green), providing status information on the netX500, as this LED is connected between the RDY and RUN pins of the chip.

Depending on the corresponding status register of the netX500, this LED can either show yellow (RDY= 0, RUN=1) or green (RDY=1, RUN=0) colour. If both pins are low or high, the LED will be off.

When the board is configured to start in “Bootstart” mode (see chapter 2.1), the LED will flash in yellow colour.

3.3 Watchdog/Reset Out

The Watchdog Out pin and the Reset Out pin of the netX are connected to two yellow LEDs (V5 and V6) which are located in the middle of the lower edge of the NXDB500-SYS and are labelled accordingly. These LEDs are lit, whenever the corresponding signal has low level.

4 Optional Extensions

4.1 DIMM-PC / Memory Board

In order to provide a simple way to evaluate the virtual DPM and the Extension Bus of the netX500, the NXDB500-SYS is equipped with a DIMM socket (X60) that can either accomodate a DIMM-PC or Hilscher specific memory modules.

For DPM evaluation, the DIMM-PC EC from GESYTEC should be used.

In that case, two more connectors on the NXDB500-SYS become active:

Connector X62, an RJ-45 jack, located on the lower edge of the board, near the left corner, which allows connecting a 10/100 Mbit Ethernet cable to the network port of the DIMM-PC.

The second connector is X63, a standard 9-pin male SUB-D connector, located right next to X62, which provides access to the serial port (RX,TX,RTS,CTS) of the DIMM-PC.

Other DIMM-PC products may also work on the NXDB500-SYS but have not been evaluated and are hence to be used at the users own risk! (On the NXDB500-SYS, the signalling voltage oft the netx500 Hostinterface has been fixed to 3.3V, hence only DIMM-PCs with 3.3V signalling voltage may be used!)

The X60 socket can also be used to connect special memory modules from Hilscher, allowing easy evaluation of the netX500 Extension Bus.

Note ***Standard memory modules (SO-DIMM) as used in laptop computers are NOT compatible with the NXDB500-SYS and must NOT be plugged to the board !***

4.2 FieldBus Addon Board

To allow future or user specific Fieldbus interfaces to be evaluated with the NXDB500-SYS, the board is equipped with a standard 0.254mm 22 pin header, allowing an Addon board to be connected to the XMAC2 port of the netX500. See chapter 5 for the pinout of this connector.

Note ***If an Addon board is used, ALL fieldbus jumpers (see chapter 2.6) must be removed!***

4.3 Prototyping Area

Directly below the TFT display, the NXDB500-SYS provides a Prototyping Area with several through hole and SMD pads, as well as a TSOP20 landing pattern. This area can be used to quickly add user specific hardware to the board without the need of developing and connecting addon boards. The Area also provides power (3.3V) and ground terminals (5 each) and access to the XMAX2 port signals.

Note ***If any user specific hardware is connected to the XMAC2 port signals, ALL fieldbus jumpers (see chapter 2.6) must be removed!***

4.4 Signal Headers

The NXDB500-SYS provides direct access to almost any signal of the netX500 through a total of 5 headers (T1 – T5) either for measurement purposes or for adding user specific hardware to the board. When using any addon boards, care should be taken, that the added hardware does not collide with onboard circuits or that any complemantary onboard hardware has been disabled (Fieldbus interfaces, SPI) by appropriate jumper settings.

The following tables show the pinout of the signal headers, which are also labelled on the board:

T1

+3V3	1	2	+3V3
T_RXD2 / GPIO8	3	4	T_TXD2 / GPIO9
T_CTS2 / GPIO10	5	6	T_RTS2 / GPIO11
T_RXD1 / GPIO4	7	8	T_TXD1 / GPIO5
T_CTS1 / GPIO6	9	10	T_RTS1 / GPIO7
T_RXD0 / GPIO0	11	12	T_TXD0 / GPIO1
T_CTS0 / GPIO2	13	14	T_RTS0 / GPIO3
VUSB_ONn / GPIO12	15	16	USB_OCn / GPIO13
USB_HSTn / GPIO14	17	18	MMC_INSn / GPIO15
GND	19	20	GND
XM0_TX	21	22	XM0_RX
XM0_IO0	23	24	XM0_IO1
XM1_TX	25	26	XM1_RX
XM1_IO0	27	28	XM1_IO1
XM2_TX	29	30	XM2_RX
XM2_IO0	31	32	XM2_IO1
PWM1B_U	33	34	PWM1B_Un
PWM1B_V	35	36	PWM1B_Vn
PWM1B_W	37	38	PWM1B_Wn
PWM1B_RSV	39	40	PWM1B_FAILn
PIO0	41	42	PIO1
PIO2	43	44	PIO3
FB2_LED0 / PIO4	45	46	FB2_LED1 / PIO5
FB3_LED0 / PIO6	47	48	FB3_LED1 / PIO7
GND	49	50	GND

Further see next page

T2

+3V3A	1	2	GNDA
AD0_0	3	4	U_ANA0
AD0_1	5	6	U_ANA0
AD0_2	7	8	U_ANA0
AD0_3	9	10	U_ANA0
AD1_0	11	12	U_ANA1
AD1_1	13	14	U_ANA1
AD1_2	15	16	U_ANA1-2
AD1_3	17	18	U_ANA1-3
GND	19	20	GND
A23	21	22	A22
A21	23	24	A20
A19	25	26	A18
A17	27	28	A16
A15	29	30	A14
A13	31	32	A12
A11	33	34	A10
A9	35	36	A8
A7	37	38	A6
A5	39	40	A4
A3	41	42	A2
A1	43	44	A0
MEMDR_CSn	45	46	MEMDR_WEn
MEMDR_RASn	47	48	MEMDR_CASn
GND	49	50	GND

Further see next page

T3

+3V3	1	2	+3V3
MEM_DQM0	3	4	MEM_DQM1
MEM_DQM2	5	6	MEM_DQM3
MEMDR_CLK	7	8	MEMDR_CKE
MEMSR_OEn	9	10	MEMSR_WEn
MEMSR_CS2n	11	12	MEMSR_CS1n
MEMSR_CS0n	13	14	GND
GND	15	16	GND
D0	17	18	D1
D2	19	20	D3
D4	21	22	D5
D6	23	24	D7
D8	25	26	D9
D10	27	28	D11
D12	29	30	D13
D14	31	32	D15
D16	33	34	D17
D18	35	36	D19
D20	37	38	D21
D22	39	40	D23
D24	41	42	D25
D26	43	44	D27
D28	45	46	D29
D30	47	48	D31
GND	49	50	GND

Further see next page

T4

+5V	1	2	+5V
ISA_D15	3	4	ISA_D14
ISA_D13	5	6	ISA_D12
ISA_D11	7	8	ISA_D10
ISA_D9	9	10	ISA_D8
GND	11	12	GND
ISA_A19	13	14	ISA_A18
ISA_A17	15	16	ISA_A16
ISA_A15	17	18	ISA_A14
ISA_A13	19	20	ISA_A12
ISA_A11	21	22	ISA_A10
ISA_A9	23	24	ISA_A8
ISA_A7	25	26	ISA_A6
ISA_A5	27	28	ISA_A4
ISA_A3	29	30	ISA_A2
ISA_A1	31	32	ISA_A0
ISA_SELA12	33	34	ISA_SELA13
ISA_SELA14	35	36	ISA_SELA15
ISA_SELA16	37	38	ISA_SELA17
ISA_SELA18	39	40	ISA_SELA19
GND	41	42	GND
ISA_D7	43	44	ISA_D6
ISA_D5	45	46	ISA_D4
ISA_D3	47	48	ISA_D2
ISA_D1	49	50	ISA_D0
ALE_AEN	51	52	ISA_BHEn
ISA_MEMWn	53	54	ISA_MEMRn
ISA_IOCHRDY	55	56	ISA_IRQ
ISA_CSn	57	58	MEMCS16n
PIO36	59	60	TCLK
EXTRESn	61	62	+3V3
GND	63	64	GND

Further see next page

T5

SPI_MOSI	1	2	SPI_CLK
SPI_MISO	3	4	SPI_CS0
SPI_CS1	5	6	SPI_CS2
I2C_SCL	7	8	I2C_SDA
USB_DNEG	9	10	USB_DPOS
WDG_ACT	11	12	RUN
RDY	13	14	CLKOUT
RSTOUT	15	16	GND

T6

+VS	1	2	+VS
GND	3	4	GND

Table 2: Pinout Signal Headers

5 Interface Connector Pinout

5.1 Communication Interfaces

5.1.1 PROFIBUS Connector

Isolated RS-485 interface:

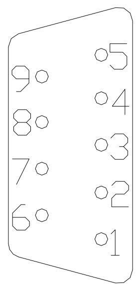

Figure 15: PROFIBUS Interface (DSub female connector)

Connection with DSub female connector	**Signal**	**Meaning**
3	RxD/TxD-P	Receive / Send Data-P respectively connection B plug
5	DGND	Reference potential
6	VP	Positive power supply
8	RxD/TxD-N	Receive / Send Data-N respectively connection A plug

Table 3: PROFIBUS Interface

5.1.2 DeviceNet Connector

Isolated ISO 11898 interface.

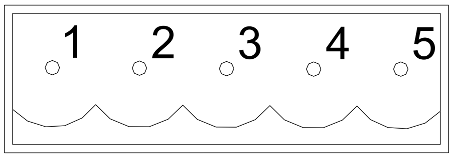

Figure 16: DeviceNet Interface (Combicon male connector, 5 pin)

Connection with Combicon male connector	Signal	Meaning
1	V-	Reference potential DeviceNet power supply
2	CAN_L	CAN Low-Signal
3	Drain	Shield
4	CAN_H	CAN High-Signal
5	V+	+24 V DeviceNet power supply

Table 4: DeviceNet Interface.

5.1.3 Interface of the AS-Interface

AS-Interface interface according IEC 364-4-41.

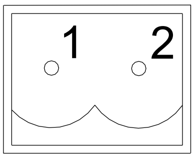

Figure 17: Interface of the AS-Interface (Combicon male connector, 2 pin)

Connection with 2 pin Combicon male connector	**Signal**	**Meaning**
1	AS-i +	AS Interface positive voltage
2	AS-i -	AS Interface negative voltage

Table 5: Interface of the AS-Interface

5.1.4 CC-Link Interface

Isolated ISO 11898 interface.

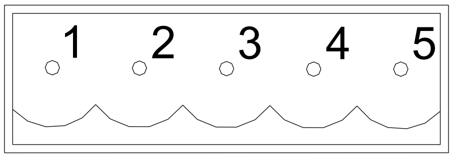

Figure 18: CC-Link Interface (Combicon Interface, 5 pin)

Combicon Interface 5 pin	Signal	Meaning
1	DA	Data A
2	DB	Data B
3	DG	Data Ground
4	SLD	Shield
5	FG	Field Ground

Table 6: CC-Link Interface

5.1.5 InterBus Interface

RS-422 interface according DIN EN 50254.

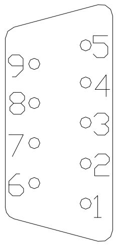

Figure 19: InterBus Interface

Connection with DSub connector male	Signal	Meaning
1	DO2	Send Data Line +
2	DI2	Receive Data Line +
3	GND2	Ground
5	Udd	Logic Voltage 5 Volt
6	/DO2	Send Data Line -
7	/DI2	Receive Data Line -

Table 7: InterBus Interface - Remote out

5.1.6 Ethernet RJ45 Plug

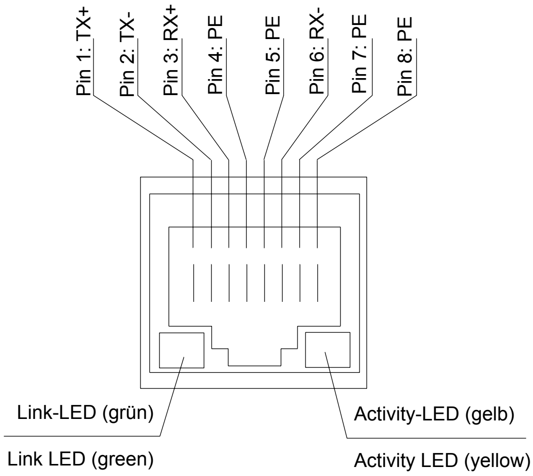

Figure 20: Ethernet Interface- Ethernet pinning at the RJ45 female connector

Pin	**Signal**	**Meaning**
1	TX+	Transmitt Data +
2	TX–	Transmitt Data –
3	RX+	Receive Data +
4	PE	connected with PE by RC circuit
5	PE	connected with PE by RC circuit
6	RX–	Receive Data –
7	PE	connected with PE by RC circuit
8	PE	connected with PE by RC circuit

Table 8: Ethernet Pinning at the RJ45 Female Connector

5.1.7 RS232 Connector

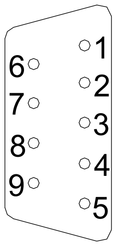

Figure 21: Communication Interface RS232

Pin	Signal	Meaning
2	RXD	Receive Data
3	TXD	Send Data
7	RTS	Ready to Send
8	CTS	Clear to Send
4	DTR	Data Terminal Ready
5	GND	Signal Ground

Table 9: Communication Interface RS232

5.1.8 USB Connector Host

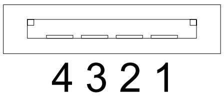

Figure 22: USB Interface female connector Type A

Pin	Name	Description
1	+5V	+5V
2	D-	Data -
3	D+	Data +
4	GND	Ground

Table 10: Pinouts

5.1.9 USB Connector Device

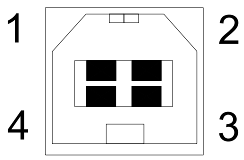

Figure 23: USB Interface female connector Type B

Pin	Name	Description
1	USB_EXT	USB Extern (+5V)
2	D-	Data -
3	D+	Data +
4	GND	Ground

Table 11: Pinouts

5.2 JTAG Connector

Pin	ARM Signals	netX Signals
1	VTref	+3.3V
2	Vsupply	+3.3V
3	nTRST	JT_TRSTn
4	GND	VSS
5	TDO	JT_TDO
6	GND	VSS
7	TMS	JT_TMS
8	GND	VSS
9	TCK	JT_TCK
10	GND	VSS
11	RTCK	Not used
12	GND	VSS
13	TDI	JT_TDI
14	GND	VSS
15	nSRST	PORn
16	GND	VSS
17	DBGRQ	Not used
18	GND	VSS
19	DBGACK	Not used
20	GND	VSS

Table 12: JTAG Connector

5.3 External LCD Connector

X52

LCD_D0	1	2	LCD_D1
LCD_D2	3	4	LCD_D3
LCD_D4	5	6	LCD_D5
LCD_D6	7	8	LCD_D7
LCD_D8	9	10	LCD_D9
LCD_D10	11	12	LCD_D11
LCD_D12	13	14	LCD_D13
LCD_D14	15	16	LCD_D15
LCD_D16	17	18	LCD_D17
GND	19	20	GND
LCD_FP	21	22	LCD_LP
LCD_CP	23	24	LCD_AC
LCD_POWER	25	26	+5V
+3V3	27	28	+3V3
GND	29	30	GND
TP_XP	31	32	TP_XM
TP_YP	33	34	TP_YM

Table 13: Pinout External LCD Connector

5.4 Power Supply

For connection to the 24 V power supply. The possible range for the power supply is 9 - 24 V.

Pin	Description
1	Ground
2	24 V

Table 14: Power Supply

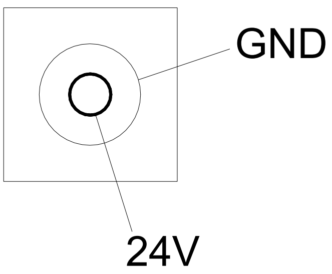

Figure 24: Power Supply

6 Lists

6.1 List of Figures

6.2 List of Tables