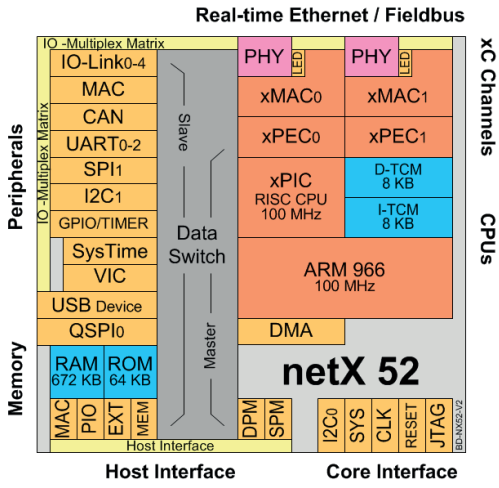
netX 52

More functions & higher Performance for Real-Time Ethernet

- Two communication channels for Real-Time Ethernet equipped with PHY or fieldbus
- Extended communication function support amongst others, PROFINET V2.3 - Dynamic Frame Packing and IO link V1.1
- Second RISC CPU for time-critical IO tasks
- Additional CAN and MAC controller
- Fast SPI host interface with Read/Write functions



Flexible „high end“ network controller equipped with a host interface or stand-alone solution for digital I/Os

Real-Time Ethernet systems are successfully used and further developed in many applications. The demands made on the resources and functionalities of network controllers are therefore increasing. The network controllers netX 51 / 52 bank on the further developed netX 50 communications architecture, which features considerably more internal storage capacity and additional function units. The netX 51 hardware is compatible with the netX 50. The netX 52 contains the same silicon, but dispenses with an external memory bus, and due to its smaller housing, is more cost-effective. These three components are thus optimized for designing modular or compact slaves, or as a Real-Time Ethernet controller on a high-performing CPU. The communication channels take all actual and future requirements from the PROFINET Specification V2.3, such as „Dynamic Frame Packing,“ into consideration. Furthermore, the new PHYs manufactured by Renesas are applied, ensuring faster throughput times and expanded diagnosis properties.

Through the internal memory for more than 670 KByte, it is possible to build together with a QSPI Flash very compact solution with twice the performance of netX 50.

For processing the fast IOs, the application is provided with a second RISC CPU. It works in parallel to ARM and significantly relieves the demands made on the ARM software via short bus cycle times. Typical applications are IO-Link Master Gateways. The xPIC takes over the IO-Link data transfer, leaving the ARM completely available for processing the transmission protocol to the master. A third Ethernet interface for connecting a PC for diagnosis and configuration purposes is implemented. Alternatively, it can also be used for connecting the netX to a host CPU. The netX then behaves like a PHY on this MII interface.

Some Real-Time Ethernet systems use the CANopen object models or the same communication services such as EtherNet/IP and DeviceNet. This results in the task of connecting CAN as the „legacy“ network to the Real-Time Ethernet system. Up to now, that entailed using an expensive netX 100 controller, with its three communication channels. As an alternative, a dedicated CAN controller is now available.

With this possibility, the netX 51 / 52 is so much more than just a Real-Time Ethernet interface chip equipped with a dual-port memory.

→ QR Code Link: netX 52
Service-Hotline: +49 (0) 6190 9907-90
www.hilscher.com

empowering communication

Product information

Technical Data

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Processor	ARM 966E-S, 100 MIPS, ARMv5TE instruction set with DSP extension, timer, interrupt and DMA controller xPIC, 32-bit RISC, 100 MIPS, TCM: 8 KByte data, 8 KByte commands
RAM	672 KByte
ROM	64 KByte with bootloader
Ports	2 × 10BASE-T / 100BASE-TX, half/ full duplex, IEEE 1588 time stamp
PHY	Integrated, auto-negotiation, auto-crossoverer
Real-Time Ethernet	EtherCAT with eight FMMUs and eight sync managers, EtherNet/IP, Modbus IDA, POWERLINK with integrated hub, PROFINET RT and IRT with integrated switch, according to PROFINET V2.3, SERCOS, VARAN
Fieldbus	The systems can be freely combined. AS-Interface (Master), CANopen (Master and Slave), CC-Link (Slave), DeviceNet (Slave), PROFIBUS (Slave)
IO-Link Controller	4 channels, data link layer control via xPIC, IO-Link V1.1
MII-Interface	Configurable in PHY or MAC mode, DMA support for Ethernet frames, HAL API operates with xPIC
CAN Controller	SJA1000 compatible
IEEE 1588 system time	32-bit second counter, 32-bit nanosecond counter
USB	Revision 1.1, 12 MBaud full speed, device mode
UART	16550 compatible, max. 3 MBaud, RTS / CTS support, Quantity 3
I²C	Master and Slave mode, 50 KHz up to 3.4 MHz, 16-bit FIFO, Quantity 2
SPI / SQI with XiP	Master and Slave mode, max. 10 MHz, 3 chip-select signal, Quantity 1 / 1
General IOs	As multiplex matrix of the internal periphery controller / 3.3 V / 6 mA, Quantity 24
Status LEDs	2 LEDs dual colored, 3.3 V / 9 mA, Quantity 2
Dual-Port Memory Mode	In part, the modes can be operated in parallel with an 8- or 16-bit data bus range. 8 / 16 / 32-bit data bus, 64 KByte configurable in 8 blocks, emulated via internal RAM
Extension-Mode	8 / 16 / 32-bit data bus, 24-bit address bus, adjustable bus timing
SPI-Mode	Slave with integrated Read/Write controller of the DPMs, 125 MHz
MII-Mode	Signals of the MII interface mapped in host interface
SDRAM Mode	16 / 32-bit SDRAM, max. 64 MByte
PIO-Mode	Freely programmable inputs and outputs, Quantity 53
JTAG	ARM processor and boundary scan
System cycle	100 MHz
Signal level	+3.3 V
Power supply	for the core: +1.5 V | for inputs/outputs: +3.3V
Operating temperature	without heat sink: -40 ... +70 °C | with heat sink 10°/W: -40 ... +85 °C
Storage temperature	-65 ... +150 °C
Power consumption	PHYs switched off, typically: +0.8 W | PHYs switched on, typically: +1.5 W
Housing	PBGA, 1 mm raster: 244 Pins
Dimensions (L x W)	15 × 15 mm

Note: All technical data may be changed without further notice.

Product Overview

NETX 52
2232.001 | netX 52 Network Controller*

** When using a Hilscher Master Protocol, a Master license must be separately ordered. It will be delivered in the form of a Security EPROMs, and is foreseen for the design. For further information, please refer to www.hilscher.com*