netX 50

Industrial Ethernet SoC - networX on Chip

- **Two communication channels as Real-Time Ethernet with PHY or fieldbus**

- **New system architecture optimized for communication and high data throughput**

- **32-Bit/200 MHz CPU ARM 966 with 112 KB SRAM / 64 KB ROM and extensive periphery**

- **Dual-Port-Memory, Extension bus or digital I/Os**

- **IO-Link Controller, 8 channels and CCD-Sensor Controller**
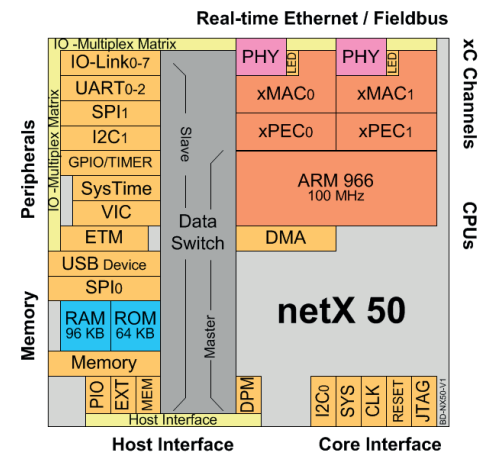
Flexible "high end" network controller with host interface or single chip solution for digital I/Os

The netX is a highly integrated network controller with a new system architecture optimized for communication and maximum data throughput.Via an integrated dual-port memory it works as an companion chip to a host CPU and realises the complete scope of industrial communication from fieldbus systems up to the Real-Time Ethernet systems. Allows the application no own CPU the host interface can be configured as Extension Bus or directly as digital input and output. The 32-Bit CPU ARM 966E-S is clocked with 200 MHz and has 112 KB internal RAM and 64 KByte ROM memory. The memory can be expanded flexible by the 32-Bit memory controller with SDRAM, SRAM or FLASH externally. Extensive periphery functions, serial interfaces such as UART, USB, SPI, I²C, as well as the integrated IO-Link and CCD controller allows a large scope of applications. The central data switch and the free configurable communication channels with its own intelligence are the unique selling proposition of the netX as an "high end" network controller.

The data switch connects via five data paths to the ARM CPU and the communication, Host and DMA controllers with the memory or the peripheral units. In this way the controllers transmit their data in parallel, contrary to the traditional sequential architecture with only one common data bus and additional bus allocation cycles.

The controllers of the two communication channels are structured on two levels and are identical to each other. They consist of dedicated ALUs and special logic units that receive their protocol functions via Microcode. For Ethernet the PHYs are integrated which means that the external circuit for Ethernet is reduced to passive componets: transformer and RC components. The Medium-Access-Controller xMAC sends or receives the data according to the respective bus access process and encrypts or converts these into Byte depictions. The Protocol Execution Controller xPEC compiles these into data packets and controls the telegram traffic. Large data amoutns are exchanged in DMA blocks over the memory of the ARM. In addition, every channel has a Dual-port-memory available for status information. Alternatively a triple buffer logic is implemented for a conflict free data exchange which always gives the address of the next free buffer.

With the intelligent communication ALUs, the netX carries out the most varied protocols and protocol combinations on one chip – an absolutely new feature in industrial communication technology.

hilscher
COMPETENCE IN
COMMUNICATION

www.hilscher.com

PRODUCT INFORMATION
TECHNICAL DATA

Technical Data	
Processor	ARM 966E-S, 200 MIPS, ARMv5TE-command set with DSP-extension
Tightly coupled memory	8 KByte Data, 8 KByte Instruction
RAM	96 KByte
ROM	64 KByte with Bootloader
Ports	2x 10BASE-T / 100BASE-TX, Half- / Full-Duplex, IEEE 1588 time stamp
PHY	Integrated, Auto-Negotiation, Auto-Crossover
Real-Time Ethernet	EtherCAT with eight FMMUs and eight Sync-Manager, EtherNet/IP, Modbus IDA, POWERLINK with integrated Hub, PROFINET RT and IRT with integrated Switch, SERCOS-III, VARAN
Fieldbus	The systems can be combined as desired. AS-Interface (Master), CANopen (Master and Slave), CC-Link (Slave), CompoNet, DeviceNet (Master and Slave), PROFIBUS (Master and Slave)
IO-Link Controller	8 Channels, automatically direction control
CCD-Sensor Controller	max. 50 MHz, 640x480 Pixel, free configurable data format
IEEE 1588 System Time	32-Bit second counter, 32-Bit Nano second counter
USB	Revision 1.1, 12 MBaud Full-Speed, Host- or Device-Mode
UART	16550 compatible, max. 3 MBaud, RTS/CTS support, Quantity 3
SPI	Master- and Slave-Mode, max. 10 MHz, 3 Chip-Select-Signals
General I/Os	3.3 V / 6 mA, Quantity 32
Status LEDs	2 LEDs two-colors, 3.3 V / 9 mA
Memory bus	32-Bit-Databus / 24-Bit-Address bus
Address region	256 MByte SDRAM / 64 MByte Flash
Memory modules	SDRAM, SRAM, Flash
Dual-Port-Memory-Mode	8 / 16 / 32-Bit-Databus, 64 KByte configurable in 8 Blocks, emulated by internal RAM
Extension-Mode	8 / 16-Bit-Databus, 24-Bit-Address bus, Bustiming adjustable
PIO-Mode	Freely programmable Inputs and Outputs, Quantity 53
JTAG	ARM-Processor and Boundary-Scan
ETM	Embedded Trace Macrocell, ETM9 V2 Medium Size
System cycles	200 MHz ARM / 100 MHz Periphery
Signal level	+3.3 V
Power supply	for Core: +1.5 V	for Input/Output: +3.3V
Operating temperature	without heat sink: -40 ... +70 °C	with heat sink 10°/W: -40 ... +85 °C
Storage temperature	-65 ... +150 °C
Power consumption	PHYs switched off: +0.8 W	PHYs switched on: +1.2 W
Housing	PBGA, 1 mm raster: 324 Pins
Dimensions (L x W)	19 x 19 mm

Note: All technical data may be changed without further notice.

Article Overview

NETX 50

2230.000 | netX 50 Network Controller*

* For application Hilscher master protocol a master license must be ordered separately. These will delivered as Security EPROMs and is provided in the design. Further information: www.hilscher.com/netx

Hilscher News: 🌐 hilscher.com   in hilscher-automation   ▶ HilscherAutomation   @HilscherAutomat