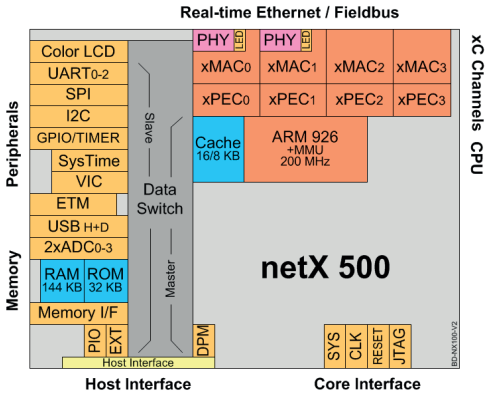
netX 100/500

Industrial Ethernet SoC for Master and Slave applications

- Four communication channels as Real-Time Ethernet or fieldbus interface individually configurable
- New system architecture optimized for communication and high data throughput
- 32-bit/200MHz CPU ARM 926 with 200 MIPs computing power for Windows CE and Linux
- Dual-port memory, AD converter and graphic controller on chip



Flexible “high end” network controller or highly integrated single chip solution for applications and communication

The netX is a highly integrated network controller with a new system architecture optimized for communication and maximum data throughput.

Based on the 32-bit CPU ARM 926EJ-S cycled at 200 MHz, it possesses a memory management unit, caches, DSP and Java extensions. The internal memory of 144 KByte RAM and 32 KByte ROM that contains the Bootloader is sufficient for smaller applications whereas for Windows CE and Linux it is supplemented with the 32 bit Memory Controller memory externally with SDRAM, SRAM or FLASH. The connection to a primary Host is carried out via the Dual-port memory interface, which is configurable for stand-alone applications also as a 16 bit extension bus. Comprehensive peripheral functions, serial interfaces such as UART, USB, SPI, I^2C as well as the integrated graphic controller permit a wide spectrum of applications. Yet, it is the central data switch and the four freely configurable communication channels with their own intelligence that is the main characteristic of the netX as a „high end” network controller.

The data switch connects via five data paths to the ARM CPU and the communication, graphic and Host controllers with the memory or the peripheral units.

In this way the controllers transmit their data in parallel, contrary to the traditional sequential architecture with only one common data bus and additional bus allocation cycles.

The controllers of the four communication channels are structured on two levels and are identical to each other. They consist of dedicated ALUs and special logic units that receive their protocol functions via Microcode. Two channels posses an additional integrated PHY for Ethernet. The Medium-Access-Controller xMAC sends or receives the data according to the respective bus access process and encrypts or converts these into Byte depictions. The Protocol Execution Controller xPEC compiles these into data packets and controls the telegram traffic. These are exchanged in DMA blocks over the memory of the ARM. In addition, every channel has a Dual-port memory available for status information or as local data picture.

With the intelligent communication ALUs, the netX carries out the most varied protocols and protocol combinations and can synchronize them independently of the reaction time of the CPU – an absolutely new feature in industrial communication technology.

→ QR Code Link: netX 100/500
Service-Hotline: +49 (0) 6190 9907-90
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Product information

Technical Data

Technical Data	
Processor	ARM 926EJ-S, 200 MIPS, ARMv5TE-command set with DSP- and Java-extension
Cache	16 KByte commands / 8 KByte Data
Tightly coupled memory	8 KByte Data
Memory Managment Unit	Windows CE- and Linux-Support
RAM	144 KByte, of this 16 KByte with external voltage supply
ROM	32 KByte with Bootloader
Ports	2x 10BASE-T/100BASE-TX, Half-/Full-Duplex, IEEE 1588 time stamp
PHY	Integrated, Auto-Negotiation, Auto-Crossover
Real-Time Ethernet	EtherCAT with three FMMUs and four Sync-Manager, EtherNet/IP, POWERLINK with integrated Hub, PROFINET RT and IRT with integrated Switch, SERCOS-III, VARAN
Fieldbus	The systems can be combined as desired. (Quantity netX 100: 1 | Quantity netX 500: 2) AS-Interface (Master), CANopen/DeviceNet (Master & Slave), CC-Link (Slave), PROFIBUS (Master & Slave)
Color-LCD-Controller	TFT-panels, Color-STN- & Mono-STN, Resolution 320 × 200 to 640 × 480, color depth 1/2/4/8/16-bit (netX 500)
Real-Time clock	With external voltage supply (netX 500)
IEEE 1588 System Time	32-bit second counter, 32-bit Nano second counter
USB	Revision 1.1, 12 MBaud Full-Speed, Host- or Device-Mode
UART	116550 compatible, max. 3 MBaud, RTS/CTS support, Quantity 3 / 3
I²C	netX 100 and netX 500
SPI	Master- and Slave-Mode, max. 10 MHz, 3 Chip-Select-Signals
AD-Converter	2 × 4 channels with 1MS/s Sample&Hold and 10 bit-resolution, Single ended, Common Analog Ground, external reference voltage
PWM	0–20 kHz/12-bit-resolution 0–80 kHz/10-bit-resolution
Encoder	2 channels, Impuls quadruplication, digital input filter
General I/Os	3.3 V/6 mA, Quantity: 16 / 16
Status LEDs	2 LEDs two-colors, 3.3 V/9 mA
Memory bus	32-bit-Databus / 24-Bit-Address bus
Address region	256 MByte SDRAM / 64 MByte Flash
Memory modules	SDRAM, SRAM, Flash
Dual-Port-Memory-Mode	8/16-bit-Databus, 64 KByte configurable in 8 Blocks; emulated by internal RAM
Extension-Mode	8/16-bit-Databus, 24-bit-Address bus, Bustiming adjustable
PIO-Mode	Freely programmable Inputs and Outputs, Quantity 53 / 53
JTAG	ARM-Processor and Boundary-Scan
ETM	Embedded Trace Macrocell, ETM9 V2 Medium Size
System cycles	200 MHz ARM / 100 MHz Periphery
Signal level	+3.3 V
Power supply	for core: +1.5 V | for Input/Output: +3.3V
Operating temperature	without heat sink: -40 ... +70 °C | with heat sink 10°/W: -40 ... +85 °C
Storage temperature	-65 ... +150 °C
Power consumption	PHYs switched off: +1.0W | PHYs switched on: +1.5 W
Housing	PBGA, 1 mm raster: 345 Pins
Dimensions (L x W)	22 × 22 mm

Note: All technical data may be changed without further notice.

Product Overview		
NETX 100	2220.000	netX 100 Network Controller*
NETX 500	2210.000	netX 500 Network Controller*

* For application Hilscher master protocol a master license must be ordered separately. These will delivered as Security EPROMs and is provided in the design. Further information: www.hilscher.com/netx

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empowering communication

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